

Quantum Algorithm for Elliptic Curve Discrete Logarithms with Space-Efficient Point Addition^{*}

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Abstract

The Elliptic Curve Discrete Logarithm Problem (ECDLP) is a fundamental problem in cryptography, and reducing the resource requirements of quantum algorithms for solving ECDLP is an important goal. In this work, we present a space-efficient quantum algorithm for solving the ECDLP over prime fields, achieving an implementation with only $3n + 6\lceil\log_2 n\rceil + O(1)$ logical qubits and $919n^3/\log_2 n + O(n^2)$ Toffoli gates, where n is the bit-length of the prime. For a 256-bit prime-field curve, our construction requires only 835 logical qubits, reducing the previous best estimates of 1098 and 1175 logical qubits by Chevignard et al. [EUROCRYPT 2026] and Babbush et al. [ArXiv Preprint 2026], respectively.

The key to our improvement is a new space-efficient reversible modular inversion circuit, which addresses the dominant space bottleneck in affine-coordinate point addition. Starting from the extended Euclidean algorithm (EEA), we refine the register-sharing technique of Proos and Zalka by introducing length registers and location-controlled arithmetic to compactly store and update intermediate variables. We further optimize the reversible update procedures and construct the corresponding controlled arithmetic circuits, resulting in a modular inversion circuit implemented by only $2n + 6\lceil\log_2 n\rceil + O(1)$ logical qubits and $195n^2 + O(n\log_2 n)$ Toffoli gates. This modular inversion circuit together with mid-circuit measurements and classical feed-forward operations provides a space-efficient controlled affine point-addition circuit and a complete implementation of Shor's algorithm for ECDLP.

^{*}This paper supersedes our earlier preprint [arXiv:2604.02311](https://arxiv.org/abs/2604.02311). Compared with the earlier version, the present paper reduces the space complexity from $5n + O(\log_2 n)$ to $3n + O(\log_2 n)$ for affine point addition and from $3n + O(\log_2 n)$ to $2n + O(\log_2 n)$ for modular inversion. It also improves the overall Toffoli counts of ECDLP from $O(n^3)$ to $O(n^3/\log n)$.

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1 Introduction

Elliptic curve cryptography (ECC), first proposed in the mid-1980s as an alternative framework for public-key cryptography [Kob87, Mil85], has become one of the foundational primitives in modern cryptographic systems. The security of ECC-based cryptosystems relies on the computational difficulty of the Elliptic Curve Discrete Logarithm Problem (ECDLP). Specifically, given an elliptic curve defined over a finite field, a base point P on that curve, and another point Q resulting from scalar multiplication of P by an unknown integer m , the ECDLP asks for the recovery of the scalar m from the two points. Despite decades of research, no classical algorithm is known that solves the ECDLP in polynomial time of bit length; the best generic attacks, such as Pollard’s rho method, require $\Theta(\sqrt{p})$ group operations, where p denotes the field size of the curve which is exponentially large [GG16].

Compared to classical public-key systems such as RSA [RSA78] and finite-field Diffie-Hellman [DH76], ECC offers equivalent security with substantially smaller key sizes. For example, according to NIST recommendations [BD20], a 256-bit elliptic curve provides a security level of 128 bits, which is comparable to that of RSA with a 3072-bit modulus. This efficiency advantage has led to the widespread adoption of ECC in both theoretical cryptographic constructions and real-world applications. Specifically, ECC is used for key exchange [DH76] and digital signature schemes [ElG85, JMV01] in widely deployed protocols, including transport layer security [BWBG⁺06], secure shell [SG09], as well as cryptocurrencies such as Bitcoin [BWQ99, NB08].

In contrast to the computational hardness of ECDLP on classical computers, the security landscape changes fundamentally in the presence of large-scale quantum computers. In 1994, Shor gave polynomial-time quantum algorithms for integer factorization and discrete logarithms [Sho94]. Because the ECDLP is a discrete-logarithm problem in a cyclic subgroup of an elliptic-curve group, it can be efficiently solved quantumly by Shor’s algorithm whenever the elliptic-curve group operation can be implemented efficiently. Proos and Zalka subsequently developed an implementation with resource analysis for prime-field elliptic curves [PZ03]. Thus, sufficiently large fault-tolerant quantum computers would break conventional ECC based on the hardness of the ECDLP. At the same time, the practical implementation of quantum algorithms for cryptography problems remains severely constrained by the limitations of near-term quantum hardware. For instance, implementing Shor’s algorithm at cryptographically relevant scales requires a fault-tolerant quantum computer with a large number of logical qubits and circuits, as well as sufficiently low physical error rates (or equivalently, achievable logical error rates after error correction) [GE21, Gid25].

Motivated by these challenges, a substantial body of work has focused on reducing the quantum resource requirements of Shor’s algorithm for integer factorization [Reg25, RV24, KMRVvK25, CFS25] and the ECDLP [RNSL17, HJN⁺20, GYCM25, KJW⁺26, CFS26, BZG⁺26, Sch26]. In recent studies, three primary resource metrics have received the most attention: (i) space, measured by the number of logical qubits; (ii) quantum gate complexity; and (iii) circuit depth. These resources are strongly coupled, and optimizing one metric often leads to increased costs in others [RNSL17, HJN⁺20, BZG⁺26, Sch26]. For each single metric, the state-of-the-art results are:

- In terms of space complexity, Chevignard, Fouque, and Schrottenloher [CFS26] proposed a low-space

variant of Shor’s ECDLP algorithm based on residue-number-system arithmetic and compressed projective-coordinate outputs. Their construction achieves the state-of-the-art asymptotic qubit complexity among existing implementations, requiring only $3.12n + O(\sqrt{n})$ logical qubits for an n -bit prime field. However, this reduction in space comes at the cost of a sufficiently larger gate count of $\tilde{O}(n^4)$.

- In terms of gate complexity, Babbush et al. [BZG⁺26] reported substantially improved resource estimates for solving ECDLP of the curve secp256k1 using 1191 logical qubits and $2^{26.27}$ Toffoli gates in the space-optimized setting, or 1441 logical qubits and $2^{25.94}$ Toffoli gates in the gate-optimized setting. However, their circuit-level details are not publicly disclosed. Schrottenloher [Sch26] subsequently gave an explicit and reproducible point addition architecture with comparable performance and slightly smaller Toffoli counts for secp256k1.
- In terms of circuit depth, Kim et al. [KJW⁺26] developed depth-optimized point-addition circuits based on QCSA-based Montgomery multiplication and low-depth binary-EEA inversion. They achieved the lowest circuit depth with adequate ancilla qubits. In terms of the product of qubit count and full depth, their qubit-optimized version achieves a 37%–40% improvement compared to the previous result by Häner et al. [HJN⁺20].

In this work, we study the space complexity of ECDLP. In particular, our focus is the modular inversion subroutine, which is the dominant source of workspace in affine-coordinate point addition. Our goal is to answer the following question:

Can the quantum space requirements for solving the ECDLP be further reduced in practice?

1.1 Contributions

The idea of reducing the space complexity of quantum ECDLP algorithms can be traced back to Proos and Zalka [PZ03], who introduced a register-sharing strategy and obtained an asymptotic space bound of $5n + O(\sqrt{n})$ for solving the ECDLP over an n -bit prime field. However, their analysis was given at a high level of abstraction and did not provide explicit reversible circuit constructions or detailed resource estimates; in particular, issues such as reversible implementation and ancilla management were not fully addressed, and the approximate treatment of modular inversion introduces a fidelity loss of $O(n^{-1})$.

Our main contribution is to turn this low-space strategy into an exact and fully explicit circuit-level construction. Since modular inversion is the dominant contributor to the overall space, we focus on designing a more space-efficient reversible implementation of this component. Building on the algorithmic framework and register-sharing idea of Proos and Zalka, we refine the representation of the EEA state, introduce length registers and location-controlled arithmetic, and provide explicit circuit constructions with detailed resource estimates. As summarized in Table 1, our construction achieves the best asymptotic logical-qubit complexity reported so far for ECDLP in the standard quantum circuit model.

Second, we provide resource estimates for our quantum circuit implementation. Specifically, we show that a modular inversion circuit can be implemented using at most $195n^2 + O(n \log_2 n)$ Toffoli gates and $247n^2 + O(n \log_2 n)$ CNOT gates. By integrating this modular inversion circuit into an affine point

Reference	Space of point addition	Space of modular inversion
[RNSL17]	$9n + 2\log_2 n + O(1)$	$7n + 2\log_2 n + O(1)$
[HJN ⁺ 20]	$8n + 10.2\log_2 n + O(1)$	$7n + \log_2 n + O(1)$
[CFS26]	$3.12n + o(n)$	not based on modular inversion
[Sch26]	$4.12n + O(\sqrt{n})$	$2.12n + O(\sqrt{n})$
This work	$3n + 6\log_2 n + O(1)$	$2n + 6\log_2 n + O(1)$

Table 1: Comparison of the number of logical qubits required for ECDLP and modular inversion.

addition circuit with mid-circuit measurement (Figures 15 and 14), we obtain a complexity of $914n^2 + O(n\log_2 n)$ Toffoli gates per point addition. Furthermore, incorporating the point addition circuit into the complete quantum algorithm for solving the ECDLP using the signed-window technique [HJN⁺20, Section 5.1] yields a total Toffoli-gate complexity of $919n^3/\log_2 n + O(n^2)$.

We complement the asymptotic comparison with numerical gate-count estimates and concrete secp256k1 resource estimates. Figure 1 reports the Toffoli and CNOT counts of our modular-inversion and point-addition circuits as functions of the field size n and Table 2 compares the resulting secp256k1 estimates with recent quantum ECDLP implementations. **For secp256k1, our construction uses 835 logical qubits, saving more than 250 logical qubits** compared to 1098 qubits in the previous best space-optimized estimate of Cheignard et al. [CFS25]. Furthermore, our Toffoli count is two orders of magnitude lower than [CFS25].

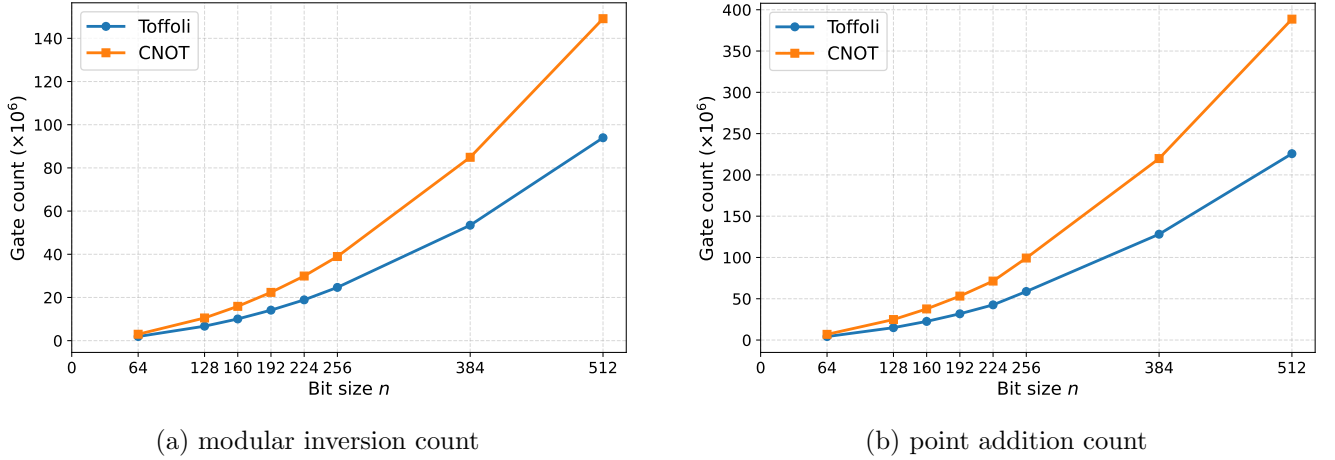


Figure 1: Toffoli gate count and CNOT gate count for modular inversion and point addition.

1.2 Overview

We present an overview of our quantum circuit for solving ECDLP. The standard implementation of Shor’s algorithm consists of $2n + 2$ controlled elliptic-curve point additions followed by a quantum Fourier transform (QFT), as illustrated in Figure 2. Replacing the QFT with its semiclassical variant reduces the logical-qubit requirement without altering the algorithmic functionality, as shown in Figure 3.

Reference	Type	Qubits	Toffolis
[BZG ⁺ 26]	Space-optimized for secp256k1	1175	$2^{26.27}$
	Gate-optimized for secp256k1	1425	$2^{25.94}$
[Sch26]	Space-optimized for secp256k1	1192	$2^{26.11}$
	Gate-optimized for secp256k1	1446	$2^{25.78}$
[CFS26]	Space-optimized for secp256k1	1098	$2^{38.10}$
This work	Space-optimized for secp256k1	835	$2^{30.63}$

Table 2: Comparison of the concrete costs of circuits for secp256k1.

Each elliptic-curve point addition is decomposed into reversible modular arithmetic operations, including modular addition, multiplication, squaring, and division, etc. Among these, modular division is the dominant contributor to the logical-qubit cost. Figure 14 illustrates the structure of our point-addition circuit, where these operations are encapsulated as modular arithmetic blocks. In particular, the in-place modular division block is realized by the circuit shown in Figure 15, which consists of a forward execution of the extended Euclidean algorithm (EEA) for modular inversion, followed by its uncomputation.

We present each component from a top-down perspective as follows.

Space-efficient reversible algorithm for modular inversion (Section 3). Our modular inversion procedure, based on the EEA, is designed to implement the following quantum transformation:

$$|x\rangle_X |0\rangle_A |0\rangle_S \mapsto |x^{-1} \bmod p\rangle_X |0\rangle_A |\Gamma(x)\rangle_S, \quad x \in \mathbb{F}_p^\times, \quad (1)$$

where A is an n -qubit workspace register, S denotes the remaining ancillary registers, and $|\Gamma(x)\rangle$ is the forward EEA state retained for later uncomputation.

We first revisit the four-phase framework of Proos and Zalka [PZ03] (see Section 3.1), which is well suited for quantum implementation because the number of iterations (which we refer to as steps) is linear in n . Rather than relying on the (inaccurate) $4.5n$ upper bound stated in [PZ03], we establish a rigorous bound showing that a complete execution of the EEA requires at most $4\lceil cn \rceil$ steps for every input x , where $c = 1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$.

Section 3.2 then develops an explicit and refined register-sharing strategy at the algorithmic level. In the original construction of [PZ03], a uniform register allocation is used to accommodate all inputs $x \in \mathbb{F}_p$ in superposition. This worst-case allocation incurs an $O(\sqrt{n})$ space overhead and necessitates truncating rare outlier cases, introducing an $O(n^{-2})$ fidelity loss. In contrast, we present an exact allocation scheme that guarantees a deterministic register bound for all inputs $x \in \mathbb{F}_p$. This reduces the additional space overhead to $O(\log n)$ while preserving exact correctness.

Finally, starting from a baseline reversible realization of this space-efficient EEA, we introduce a sequence of algorithmic optimizations in Section 3.3 that reorganize the update rules and eliminate redundant arithmetic operations. We provide complete pseudocode (Algorithm 3) together with representative

classical execution traces (Table 4), which illustrate the reversibility and correctness of each step and clarify how the procedure can be translated into a quantum circuit.

Explicit quantum circuit construction for modular inversion (Section 4). To show that our modular inversion algorithm admits an explicit quantum circuit implementation, we present a detailed construction based on Algorithm 3. We begin with the overall circuit architecture (Figures 5 and 6 in Section 4.1), where location-controlled operations arise as key non-standard components.

Before giving their explicit implementations, we establish the necessary tools. In Section 4.2, we introduce step-dependent active windows, which restrict the relevant index range at each step and thereby reduce gate complexity. We then introduce unary iteration (Section 4.3) as a primitive for implementing controlled indexed operations, which enables the realization of these location-controlled components.

Finally, in Section 4.4, we present explicit constructions of the location-controlled circuit blocks, including swap, addition/subtraction, and length-update operations (Figures 9, 10, 12, and 13). In addition to the circuit diagrams, we provide detailed explanations of the underlying techniques and design rationale.

Affine point addition with mid-circuit measurements (Section 5). We further show that affine point addition can be implemented using our EEA inversion circuit with only $3n + O(\log n)$ logical qubits by allowing mid-circuit measurements and classical feed-forward operations. The main issue is the in-place division step

$$|x\rangle_X |y\rangle_Y |0\rangle_A \mapsto |x\rangle_X |y/x\rangle_Y |0\rangle_A.$$

To perform this map, the EEA inversion circuit in Equation (1) is first applied to x . This requires one clean n -qubit register A and leaves the forward EEA state $\Gamma(x)$ to be cleared later. After the quotient y/x has been written into A , however, the register A is no longer clean, so the inverse EEA circuit has no available n -qubit workspace.

As shown in Figure 15, we resolve this problem by measuring the register containing the old value y in the Hadamard basis and resetting it to zero. This makes the register Y available as the clean workspace for the inverse EEA circuit, which recovers x and clears $\Gamma(x)$. This measurement is valid because, after y/x has been written into A , the old value y is redundant and can be recovered from x and y/x . Measuring $|y\rangle$ in the Hadamard basis gives a uniformly random outcome $b \in \{0, 1\}^n$, and the only effect on the remaining registers is the phase $(-1)^{b \cdot y}$. Thus measuring the register Y does not destroy coherence. The phase is removed by recomputing y from x and y/x , applying the corresponding Pauli Z corrections, and uncomputing the recomputation. The same measurement and correction procedure gives an in-place multiplication circuit. Consequently, affine point addition can be implemented using three n -qubit registers X , Y , and A , together with the $O(\log n)$ auxiliary qubits required by the EEA circuit.

We note that mid-circuit measurements have previously been used to reduce either the qubit count or the T -gate cost of quantum arithmetic circuits [Gid19, KSS25, LMNS25, KH21]. In particular, the lowest-qubit quantum algorithm currently known for the elliptic-curve discrete logarithm problem also makes extensive use of measurements to reduce the number of qubits [CFS26]. That work does not keep the full

elliptic-curve point, nor does it reduce the index registers using a semiclassical Fourier transform. Instead of computing the full point, it computes a one-bit Legendre symbol from the projective coordinates of that point using residue-number-system arithmetic. Its measurements are used to release intermediate nodes in a spooky pebbling strategy for a binary tree [Gid19, KSS25]. In contrast, we keep the standard affine point-addition structure and use measurements only inside the in-place division and multiplication blocks, where they recycle a register needed as workspace for running the inverse EEA circuit.

Resource estimations (Section 6). Putting everything together, we quantify the space complexity and gate costs of the complete construction of Shor’s ECDLP circuit. We first show in Section 6.1 that the modular inversion circuit requires $2n + 6\lfloor \log_2 n \rfloor + 19$ logical qubits, and that the affine point addition circuit of Section 5 can therefore be implemented using $3n + 6\lfloor \log_2 n \rfloor + 19$ logical qubits. Section 6.2 then combines the per-block gate costs (Section 4.4) with the step-dependent active-window bounds (Section 4.2), to obtain an upper bound of $195n^2 + O(n \log_2 n)$ Toffoli gates and $247n^2 + O(n \log_2 n)$ CNOT gates for modular inversion, as well as an upper bound of $914n^2 + O(n \log_2 n)$ Toffoli gates for one affine point addition.

We complement these asymptotic bounds with concrete circuit generation and blockwise compilation using Qiskit in Section 6.3, reporting numerical Toffoli and CNOT gate counts for prime-field sizes ranging from 64 to 512 bits. Finally, in Section 6.4, we incorporate signed-window scalar multiplication and the associated table look-ups into the complete Shor’s ECDLP circuit. This yields an overall Toffoli complexity of $919n^3 / \log_2 n + O(n^2)$. **For the secp256k1 curve, our construction requires 835 logical qubits and $2^{30.63}$ Toffoli gates.**

1.3 Open questions

Our work leaves several open questions for future investigation:

- **Gate-count optimization.** Our construction prioritizes logical-qubit efficiency and gives explicit reversible circuits for all arithmetic components. However, several building blocks, especially location-controlled arithmetic, length-register updates, and controlled modular operations, may still admit substantial improvements of their gate counts.
- **Depth analysis and space-depth trade-offs.** This paper focuses primarily on the number of logical qubits and Toffoli/CNOT gate counts, and does not provide a detailed analysis of circuit depth. A natural next step is to study the depth of our modular inversion and point-addition circuits, identify which parts of the computation can be parallelized, and quantify the resulting trade-offs between space, gate count, and depth.
- **Applications beyond elliptic-curve discrete logarithms.** We note that modular inversion is a general-purpose arithmetic primitive, not only restricted to ECDLP. It would be useful to investigate whether the space-efficient reversible EEA and register-sharing techniques developed here can improve other quantum algorithms that require modular division or inversion, such as Decoded Quantum Interferometry (DQI) [KSG+25].

- **AI-assisted discovery of quantum arithmetic circuits.** An important open question is whether AI systems can enable the automated design of quantum arithmetic circuits, supporting both the discovery of new resource-efficient circuits and the optimization of existing ones. One possible approach is to encode techniques such as windowing, unary iteration, register sharing and mid-circuit measurement as composable modules, and to develop AI-assisted evolutionary frameworks, inspired by systems such as AlphaEvolve [NV⁺25], that iteratively explore their replacement and composition under automated correctness verification and resource-aware evaluation.

2 Preliminaries

This section provides a very brief discussion of the basic concepts used in this work. We assume that readers have basic knowledge of quantum computation. For a general survey of quantum algorithms for algebraic problems, we recommend the survey written by Childs and van Dam [Cd10].

2.1 Quantum computing and the Toffoli counts

We write basis quantum states as $|x\rangle$, where x is a bit string, and we model a quantum algorithm as a circuit composed of elementary gates applied to one or more qubits. A key feature is that circuits can create and transform superpositions of basis states, enabling interference effects that are exploited by quantum algorithms.

At the fault-tolerant logical level, it is common to express circuits over a universal gate set such as Clifford+ T [NC10]. In many architectures the T gate is substantially more expensive than Clifford operations, so circuit cost is frequently summarized by T -count, T -depth, or related metrics [FMMC12]. For design and validation, however, it is often convenient to use a purely reversible gate basis.

Accordingly, we express the main reversible components as *Toffoli networks*. The Toffoli gate maps

$$|x, y, z\rangle \mapsto |x, y, z \oplus (xy)\rangle,$$

and it forms a universal primitive for classical reversible computation [NC10]. A practical benefit of working at the Toffoli-network level is that such networks admit exact realizations over Clifford+ T [AMMR13], avoiding approximation overhead associated with synthesizing arbitrary unitaries. Moreover, Toffoli-based reversible circuits can be efficiently simulated on classical inputs at scales far beyond what is possible for general quantum-state simulation, which makes testing and debugging large arithmetic circuits significantly more tractable [HRS17]. For these reasons, we specify the core arithmetic and elliptic-curve routines using Toffoli and CNOT gates.

2.2 Elliptic curves and the ECDLP

Let p be a large prime and let $\mathbb{F}_p$ denote the finite field with p elements. An elliptic curve $E/\mathbb{F}_p$ (in short Weierstrass form) is the set of affine solutions $(x, y) \in \mathbb{F}_p^2$ to an equation $y^2 = x^3 + ax + b$, together with a distinguished point $\mathcal{O}$ at infinity. The set of $\mathbb{F}_p$ -rational points, together with $\mathcal{O}$, is denoted by $E(\mathbb{F}_p)$.

The points on $E(\mathbb{F}_p)$ form an abelian group under the elliptic-curve addition law, with identity element $\mathcal{O}$. For affine points $P_1 = (x_1, y_1)$ and $P_2 = (x_2, y_2)$ that are not inverse to each other, the sum $P_3 = P_1 + P_2$ can be computed via a slope parameter λ :

$$x_3 = \lambda^2 - x_1 - x_2, \quad y_3 = \lambda(x_1 - x_3) - y_1,$$

where λ equals the chord slope $\frac{y_2 - y_1}{x_2 - x_1}$ when $P_1 \neq P_2$, and the tangent slope $\frac{3x_1^2 + a}{2y_1}$ when $P_1 = P_2$. Exceptional cases (e.g., $P_i = \mathcal{O}$ or $P_2 = -P_1$) are handled according to the standard group properties.

For an integer $m \geq 1$, the notation $[m]P$ denotes the m -fold sum of a point P with itself, i.e. $[m]P = P + P + \dots + P$, where P occurs m times. This m -fold sum can be extended to all $m \in \mathbb{Z}$ by defining $[0]P = \mathcal{O}$ and $[-m]P = [m](-P)$ for $m \geq 1$. The operation $m \mapsto [m]P$ is called *scalar multiplication* and is the core primitive used in elliptic-curve cryptography.

Let $P \in E(\mathbb{F}_p)$ generates a cyclic subgroup $\langle P \rangle$ of order r , and let $Q \in \langle P \rangle$. The *elliptic-curve discrete logarithm problem (ECDLP)* is to recover the unique $m \in \{0, 1, \dots, r-1\}$ such that

$$Q = [m]P.$$

In classical settings, the best generic algorithms require on the order of $\Theta(\sqrt{p})$ group operations [GG16], which is exponential in the bit length $\log_2 p$.

2.3 Shor's quantum algorithm for ECDLP

Shor's discrete-logarithm algorithm for solving ECDLP applies to elliptic curve over any finite abelian group and therefore to $E(\mathbb{F}_p)$. Let $n = \lfloor \log_2 p \rfloor + 1$ be the bit-length of p . The quantum procedure uses two exponent registers and one register storing an elliptic curve point.

Firstly, initialize two $(n+1)$ -qubit registers¹ to be $|0^{n+1}, 0^{n+1}\rangle$, and apply Hadamard gate to all the qubits to obtain a uniform superposition over pairs $(k, \ell) \in \{0, 1, \dots, 2^{n+1} - 1\}^2$. Next, coherently compute the elliptic curve group action into an accumulator as

$$\sum_{k, \ell=0}^{2^{n+1}-1} |k, \ell\rangle |\mathcal{O}\rangle \mapsto \sum_{k, \ell=0}^{2^{n+1}-1} |k, \ell\rangle |[k]P + [\ell]Q\rangle. \quad (2)$$

After this step, apply Quantum Fourier Transform $\text{QFT}_{2^{n+1}}$ to both exponent registers and then measure them. Finally, a classical post-processing procedure uses the measurement outcomes to reconstruct the discrete logarithm m with high probability, as shown in [Sho94].

In terms of resource, the dominant cost arises from the coherent group evaluation, i.e., the double-scalar multiplication on elliptic curve points. To reduce the qubit cost associated with QFT, its full circuit on the exponent registers can be replaced by a semiclassical variant [GN96]. This semiclassical Fourier transform performs measurements during the computation, reusing qubits and applying conditional phase rotations based on previously observed outcomes. The overall quantum circuits of Shor's algorithm for ECDLP using QFT (resp. semiclassical QFT) are shown in Figure 2 (resp. Figure 3).

¹Hasse's bound [Has36] indicates that $\text{ord}(P) \leq \#E(\mathbb{F}_p) \leq p + 1 + 2\sqrt{p}$, which can be represented by at most $n + 1$ bits.

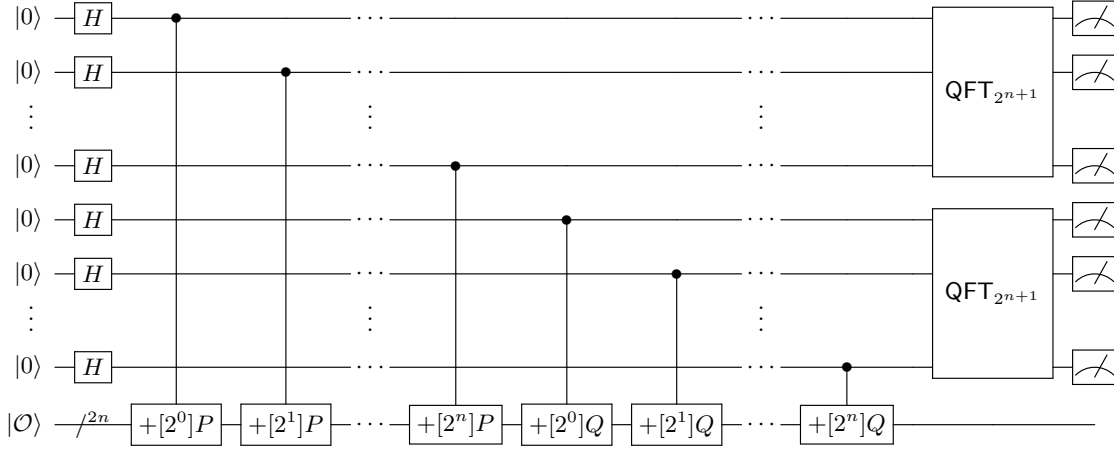


Figure 2: The overall quantum circuit of Shor's algorithm for solving ECDLP using QFT. The qubits, from top to bottom, correspond to the exponent registers containing k and ℓ in Equation 2 (ordered from lower-order bits to higher-order bits), and to the register that stores the elliptic curve point accumulator.

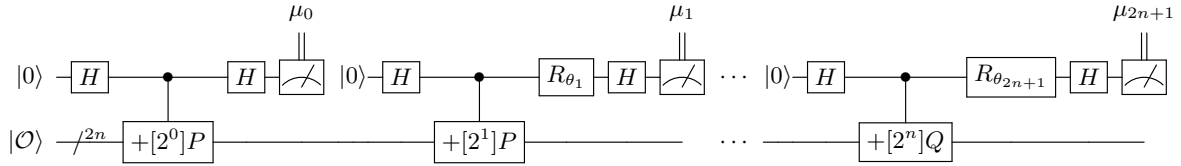


Figure 3: The overall quantum circuit of Shor's algorithm for solving ECDLP using semiclassical QFT. The gates R_{θ_i} denote rotation gates with rotation angle $\theta_i = \sum_{j=0}^{i-1} 2^{i-j} \mu_j$, where the values $\mu_j \in \{0, 1\}$ are outcomes obtained in previous measurements. By employing the semiclassical QFT, the exponent register requires only a single qubit, resulting in a reduction of $2n + 1$ qubits compared to the standard implementation.

3 Space-Efficient Extended Euclidean Algorithm

As discussed in previous sections, the dominant cost in designing quantum circuits for solving ECDLP via Shor's algorithm arises from coherent group additions on elliptic curve points. Among these operations, modular inversion is the most resource-consuming component. In this section, we present a space-efficient and reversible algorithm for modular inversion based on the Extended Euclidean Algorithm. This design is suitable for further translation into a quantum circuit, as detailed in Section 4.

Suppose that $p > x$ are two positive integers. The well-known *Euclidean algorithm* can be used to compute the greatest common divisor (GCD) of p and x . The algorithm initializes $r_0 := p$ and $r_1 := x$, and for iterations $i = 1, 2, \dots$, it repeatedly divides r_{i-1} by r_i to obtain the quotient $q_i = \lfloor r_{i-1}/r_i \rfloor$ and the remainder $r_{i+1} = r_{i-1} - q_i r_i$. The process terminates when $r_{k+1} = 0$, at which point the greatest common divisor of p and x equals r_k .

The *Extended Euclidean Algorithm (EEA)* not only computes the GCD of p and x , but also outputs the modular inverse $x^{-1} \bmod p$ when p and x are coprime. In addition to computing the sequence r_i , it also initializes $t_0 := 0$ and $t_1 := 1$, and for each iteration $i = 1, 2, \dots$, updates $t_{i+1} = t_{i-1} + q_i t_i$ after obtaining $q_i = \lfloor r_{i-1}/r_i \rfloor$. When the algorithm first encounters $r_k = 1$, the modular inverse is given by

$$(-1)^{k-1}t_k \bmod p.$$

When realizing the Extended Euclidean algorithm on a quantum computer to compute the modular inverse of x with a prime modulus p of n binary digits, the primary challenge lies in handling superpositions of x . The number of iterations required varies from 1 to $O(n)$ depending on the input, implying that a straightforward implementation would require $O(n)$ iterations. Each iteration involves divisions and multiplications on n -digit numbers, leading to an overall gate complexity of $O(n^3)$.

In what follows, we describe the dedicated four-phase algorithm framework first proposed in [PZ03], followed by our own algorithmic optimizations and the details of our optimized circuit implementation.

3.1 The four-phase algorithm framework

The four-phase algorithm framework was originally introduced in [PZ03]. It operates on six quantum registers, denoted as r_{i-1} , r_i , t_{i-1} , t_i , q_i , and ℓ , where the first five registers correspond to the variables used in the i -th iteration of EEA. To compute the quotient $q_i = \lfloor r_{i-1}/r_i \rfloor$, the algorithm performs a binary long-division procedure consisting solely of bit shifts and long additions or subtractions. The algorithm proceeds through the following four phases:

- **Phase 1.** The register containing r_i is repeatedly shifted left by one bit, while the shift counter ℓ is incremented at each step. This continues until the inequality $2^\ell r_i > r_{i-1}$ holds. Conceptually, this phase determines the largest power of two by which r_i can be multiplied without exceeding r_{i-1} . Equivalently, after the loop terminates, $\ell_0 := \ell - 1$ gives the highest bit position in the binary representation of q_i .
- **Phase 2.** The register containing r_i is then shifted right by one bit per step, with ℓ decremented accordingly. At each step, the registers corresponding to r_{i-1} and q_i are updated as

$$(r_{i-1} - q' r_i, q') \rightarrow (r_{i-1} - (q' + 2^\ell q_{i,\ell}) r_i, q' + 2^\ell q_{i,\ell}),$$

depending on whether $r_{i-1} - q' r_i$ is at least $2^\ell r_i$. Here q' denotes the current partial quotient, given by $q' = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \dots + 2^{\ell+1} q_{i,\ell+1}$, representing the most significant bits accumulated so far in the binary expansion

$$q_i = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \dots + q_{i,0}.$$

This iterative process ultimately yields the transformation

$$(r_{i-1}, 0) \rightarrow (r_{i-1} - q_i r_i, q_i),$$

completing the computation of q_i .

- **Phase 3.** The register containing t_i is shifted left by one bit per step, and ℓ is incremented correspondingly. The registers associated with t_{i-1} and q_i are updated as

$$(t_{i-1} + q'' t_i, q') \rightarrow (t_{i-1} + (q'' + 2^\ell q_{i,\ell}) t_i, q'),$$

where the update depends on the bit value $q_{i,\ell}$ of q_i . After each step, $q_{i,\ell}$ is reset to 0, depending on whether $t_{i-1} + (q' + 2^\ell q_{i,\ell})t_i > 2^\ell t_i$. Here q' and q'' represent the most and least significant portions of the quotient, respectively:

$$q' = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \cdots + 2^\ell q_{i,\ell}, \quad q'' = 2^{\ell-1} q_{i,\ell-1} + 2^{\ell-2} q_{i,\ell-2} + \cdots + q_{i,0}.$$

After completing all steps, the registers corresponding to t_{i-1} and q_i are updated as

$$(t_{i-1}, q_i) \rightarrow (t_{i-1} + q_i t_i, 0).$$

- **Phase 4.** Finally, the register containing t_i is repeatedly shifted right by one bit, and ℓ is decremented at each step. The process terminates once $\ell = 0$.

Upon completion of all four phases, SWAP operations are applied between the register pairs corresponding to (r_{i-1}, r_i) (which is currently (r_{i+1}, r_i)) and the register pairs corresponding to (t_{i-1}, t_i) (which is currently (t_{i+1}, t_i)), respectively. This completes one full iteration of the EEA implementation.

We emphasize that, during the execution of this four-phase algorithm, the correspondence between the iteration index in EEA and the phase number may vary depending on the input value x . In other words, the algorithm's internal progression through iterations and phases is input-dependent. To avoid ambiguity in the subsequent descriptions, we use “step” to represent any sub-iteration occurring within any phase of an EEA iteration. The example in Table 3 illustrates how the step status evolves for different input values under this four-phase framework.

Input	x_1	x_2	x_3
Step 1	Iteration 1, Phase 1	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 2	Iteration 1, Phase 1	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 3	Iteration 1, Phase 2	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 4	Iteration 1, Phase 2	Iteration 1, Phase 1	Iteration 1, Phase 2
Step 5	Iteration 1, Phase 3	Iteration 1, Phase 1	Iteration 1, Phase 2
Step 6	Iteration 1, Phase 3	Iteration 1, Phase 2	Iteration 1, Phase 2
Step 7	Iteration 1, Phase 4	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 8	Iteration 1, Phase 4 (and SWAP)	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 9	Iteration 2, Phase 1	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 10	Iteration 2, Phase 1	Iteration 1, Phase 2	Iteration 1, Phase 4
Step 11	Iteration 2, Phase 1	Iteration 1, Phase 3	Iteration 1, Phase 4
Step 12	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 1, Phase 4 (and SWAP)
Step 13	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 2, Phase 1
Step 14	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 2, Phase 1
Step 15	Iteration 2, Phase 3	Iteration 1, Phase 3	Iteration 2, Phase 2
Step 16	Iteration 2, Phase 3	Iteration 1, Phase 4	Iteration 2, Phase 2
...	...	...	...
Step 100	Iteration 9, Phase 3	Iteration 5, Phase 2	Iteration 8, Phase 4
...	...	...	...

Table 3: An example illustrating that the EEA iteration index and phase number may vary depending on the input value x .

Although the sequence of step statuses differs for each input x , the total number of steps required to reach an index k such that $r_{k-1} = 1, r_k = 0$ can be bounded within the interval $[4n, 4\lceil cn \rceil]$ with $c = 1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$, as formally proven in Appendix A.1. This bounded-step property is crucial for quantum implementation: it implies that a quantum circuit corresponding to one “step” can be repeated at most $4\lceil cn \rceil \approx 5.76n$ times to definitely obtain the modular inverse of any input x in superposition. Since each step involves arithmetic operations such as shifts, additions, and subtractions, which require $O(n)$ quantum gates, the overall gate complexity of the algorithm is reduced to $O(n^2)$.

Keeping the above discussion in mind, the forward space-efficient EEA subroutine for computing the modular inverse $x^{-1} \bmod p$, where p is a prime represented with n binary digits and $x \in \{1, 2, \dots, p-1\}$, is summarized in Algorithm 1. In this context: (i) the register allocation strategy is described in Section 3.2; (ii) Algorithm 3 provides the optimized stepwise iteration designed to minimize gate complexity and ensure quantum reversibility, as further discussed in Sections 3.2 and 3.3; (iii) when $x > p/2$, we run the EEA on $p - x$ instead of x and record this choice in the iteration-parity qubit.

Algorithm 1 Forward space-efficient EEA inversion subroutine

Require: Quantum registers $|x\rangle|0^n\rangle|0^m\rangle$, where the first n -qubit register is the input/output register, the second n -qubit register is a large workspace, and the remaining m qubits serve as auxiliary qubits.

Ensure: Output state $|x^{-1} \bmod p\rangle|0^n\rangle|\Gamma(x)\rangle$, where $|\Gamma(x)\rangle$ denotes the remaining forward EEA state.

Initialize register **Work1** with $(n+3)$ qubits as $|100, p\rangle$ ▷ Using $(n+3)$ auxiliary qubits

Initialize register **Work2** with $(n+3)$ qubits as $|000, x\rangle$ ▷ Pad x to n bits on the left

Initialize **Length** registers to $|\ell_t := 1, \ell_q := 0, \ell_{r'} := \text{length of } x, \ell_s := 0\rangle$

Initialize **Control** registers to $|\text{Phase1} := 0, \text{Phase2} := 0, \text{Sign} := 0, \text{Iter} := 0\rangle$

if $x > p/2$ **then** ▷ Ensures that the algorithm is invertible

Iter $\leftarrow$ **Iter** $\oplus$ 1

end if

if **Iter** = 1 **then**

$x \leftarrow p - x$

end if

for $i = 1, 2, \dots, 4\lceil cn \rceil$ **do** ▷ Main iterative loop performing the optimized algorithm steps

Execute Algorithm 3 on the quantum registers

end for

Keep the t' part of **Work2** as the output value

if **Iter** = 0 **then** ▷ Convert t' to the positive inverse modulo p

$t' \leftarrow p - t'$

end if

Reset the input-independent terminal contents of the large workspace to $|0^n\rangle$

Denote the remaining forward EEA state by $|\Gamma(x)\rangle$

3.2 Space-efficient algorithm by register sharing

In [PZ03], the authors introduced the concept of *register sharing*. The central idea of register sharing is that, during the execution of the EEA, the sequence $\{r_i\}$ is monotonically decreasing while the sequence $\{t_i\}$ is monotonically increasing. This complementary behavior allows both values to occupy the same quantum register at different stages of computation, thereby reducing the overall space requirement. The

identity

$$r_{i-1}t_i + r_it_{i-1} = p$$

implies that two quantum registers, each consisting of $(n + 2)$ qubits, are sufficient: one to store the pair (r_{i-1}, t_i) and the other to store (r_i, t_{i-1}) .

We extend this register-sharing idea further. Specifically, we observe that a single quantum register of $(n + 2)$ qubits can be used to store the triple (r_{i-1}, t_i, q_i) simultaneously, including the intermediate states that arise during phases 2 and 3 of the algorithm. These phases are responsible for computing $q_i = \lfloor r_{i-1}/r_i \rfloor$ and updating the variables

$$r_{i-1} \leftarrow r_{i-1} - q_ir_i, t_{i-1} \leftarrow t_{i-1} + q_it_i.$$

The detailed allocation of quantum registers is described as follows, and illustrated in Figure 4.

- **Work1 register (of $(n + 3)$ qubits).** The left-most $\ell_t + 1$ qubits encode the value $t := t_i$ in little-endian order (here we append a zero to the rightmost position of t in order to simplify the circuit implementation). The following ℓ_q qubits store the intermediate quotient value $q := q'$ (only the effective most significant bits) in phases 2 and 3, in big-endian order. The remaining qubits hold the value $r := r_{i-1}$ (or its updated form $r := r_{i-1} - q'r_i$) in big-endian order.
- **Work2 register (of $(n + 3)$ qubits).** The right-most $\ell_{r'}$ qubits store $r' := r_i$ in big-endian order, while the remaining qubits store the value $t' := t_{i-1}$ (and its intermediate update $t' := t_{i-1} + q''t_i$) in little-endian order. During phases 2 and 3, this register may be circularly shifted left by ℓ_s positions. In such cases, the value t' may span both ends of the register, effectively splitting into two contiguous parts.
- **Length registers.** Four auxiliary registers are used to manage variable-length storage. Each of them contains $\lfloor \log_2 n \rfloor + 1$ qubits. They store the length indicators $\ell_t, \ell_q, \ell_{r'}$, and the shift counter ℓ_s respectively. These **Length** registers mark the logical boundaries within the **Work1** and **Work2** registers and enable coherent manipulation of superposed inputs of varying lengths.
- **Control registers.** Two single-qubit **Phase** registers indicate the current phase of the four-phase algorithmic framework, and one single-qubit **Iter** register that records the parity of the current EEA iteration number. Additionally, there are two auxiliary single-qubit registers, **Sign** and **Ctrl**, used for intermediate flag and control operations.

We next describe the behavior of the system when performing comparison, addition, and subtraction operations on the register pairs (r, r') and (t, t') . The arithmetic between r and r' is relatively straightforward: a left shift by ℓ_s positions corresponds to multiplying r' by 2^{ℓ_s} . In contrast, the arithmetic involving t and t' requires a more careful interpretation. A convenient way to view this operation is that a left shift of ℓ_s positions can be regarded as dividing t' by 2^{ℓ_s} , where the integer part is placed in the left-most portion of **Work2**, and the fractional part occupies the right-most portion. When t is added to the integer part of t' (which is properly aligned), the arithmetic relation can be expressed as $2^{-\ell_s}t' + t = 2^{-\ell_s}(t' + 2^{\ell_s}t)$. Thus, the expression $t' + 2^{\ell_s}t$ represents the desired result, corresponding to a left shift by ℓ_s positions.

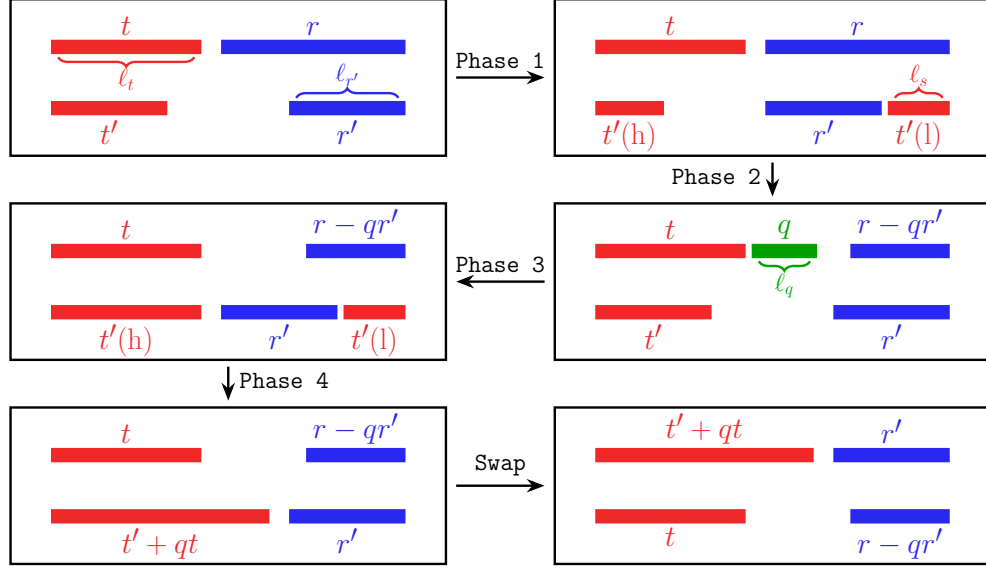


Figure 4: An illustration of how the two **Work** registers are allocated for temporary variables within a single iteration of the EEA. The upper and lower stripes represent the **Work1** and **Work2** registers, respectively. The symbols (h) and (l) indicate that the value t' is split into its higher-order bits (h) and lower-order bits (l), which are placed at the corresponding positions on the two sides of the **Work2** register.

With this register allocation, one step of our space-efficient EEA proceeds as in Algorithm 2. To illustrate how the proposed space-efficient EEA operates in practice, we also provide a concrete execution example for $p = 37$ and $x = 13$, shown in Table 4.

For each step, Table 4 shows how the contents of the two **Work** registers evolve and how different variables are mapped onto **Work1** and **Work2** under the register-sharing strategy. In particular, the variable t' stored in **Work2** is divided into two parts that occupy the left-most and right-most portions of the register. The division symbols are not explicitly implemented in the quantum circuit; they are all illustrative and inferred from the corresponding **Length** registers, used to visualize the register allocation. In the actual quantum implementation, all registers are in superposition, and the location of these division symbols may vary across different input values.

3.3 Algorithmic optimizations

The baseline implementation of one step, as described in the previous subsection, was constructed to be fully reversible, ensuring that every state transformation can be realized as a unitary operation on a quantum computer. However, this direct implementation contains multiple redundant operations that unnecessarily increase both the circuit depth and gate count. In this subsection, we present a series of algorithmic optimizations applied to the baseline design in order to reduce the quantum circuit depth and overall gate complexity.

Algorithm 2 One step of our EEA implementation with register sharing

Require: Work1 register stores $|t, q, r\rangle$, Work2 register stores $|t', r'\rangle$

Require: Length registers store $|\ell_t, \ell_q, \ell_{r'}, \ell_s\rangle$

Require: Control registers store $|\text{Phase1}, \text{Phase2}, \text{Iter}, \text{Sign}\rangle$.

```

if (Phase1, Phase2) = (0, 0) then                                ▷ Arithmetic logic for the four phases
    Perform a one-position left shift on Work2
     $\ell_s \leftarrow \ell_s + 1$ 
     $\text{Sign} \leftarrow \text{Sign} \oplus (r < 2^{\ell_s} r')$                                 ▷ Act on qubits  $(\ell_t + \ell_q + 2)$  through  $(n + 3 - \ell_s)$ 
else if (Phase1, Phase2) = (0, 1) then
    Perform a one-position right shift on Work2
     $\ell_s \leftarrow \ell_s - 1, \ell_q \leftarrow \ell_q + 1$ 
     $(\text{Sign}, r) \leftarrow (\text{Sign}, r) - 2^{\ell_s} r'$                                 ▷ Use register Sign to store the sign of the subtraction result
    if Sign = 1 then
         $r \leftarrow r + 2^{\ell_s} r'$                                 ▷ Ignore overflows
    end if
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
    Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1                                ▷ The least significant work qubit of  $q$ 
else if (Phase1, Phase2) = (1, 0) then
    Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1
    if Sign = 0 then
         $t' \leftarrow t' - 2^{\ell_s} t$                                 ▷ Act on left-most  $(\ell_t + 1)$  qubits
    end if
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
     $(\text{Sign}, t') \leftarrow (\text{Sign}, t') + 2^{\ell_s} t$                                 ▷ Use register Sign to store the sign of the addition result
    Perform a one-position left shift on Work2
     $\ell_s \leftarrow \ell_s + 1, \ell_q \leftarrow \ell_q - 1$ 
else if (Phase1, Phase2) = (1, 1) then
     $\text{Sign} \leftarrow \text{Sign} \oplus (t' \geq 2^{\ell_s} t)$                                 ▷ Same qubit range as above
    Perform a one-position right shift on Work2
     $\ell_s \leftarrow \ell_s - 1$ 
end if
if  $\ell_q = 0$  and  $\ell_{r'} > 0$  then                                ▷ Phase update logic;  $\ell_{r'} = 0$  indicates algorithm termination
     $\text{Phase2} \leftarrow \text{Phase2} \oplus \text{Sign} \oplus \text{Phase1}, \text{Sign} \leftarrow \text{Sign} \oplus \text{Phase2}$ 
end if
if  $\ell_s = 0$  then
     $\text{Phase1} \leftarrow \text{Phase1} \oplus 1, \text{Phase2} \leftarrow \text{Phase2} \oplus 1$ 
end if
if  $\ell_q = 0$  and  $\ell_s = 0$  then                                ▷ Register swapping at the end of one EEA iteration
    Swap Work1 and Work2
    Update  $\ell_t$  to the bit length of the new  $t$                                 ▷ Act on the left-most  $(n + 3 - \ell_{r'})$  qubits of Work1 and Work2
    Update  $\ell_{r'}$  to the bit length of the new  $r'$                                 ▷ Act on the right-most  $(n + 2 - \ell_t)$  qubits of Work1 and Work2
     $\text{Iter} \leftarrow \text{Iter} \oplus 1$ 
end if

```

Step	Work1	Work2	t	q	r	t'	r'	ℓ_t	ℓ_q	$\ell_{r'}$	ℓ_s	Phase1	Phase2	Iter	Sign
0	10 0100101	00000 1101	1	0	37	0	13	1	0	4	0	0	0	0	0
1	10 0100101	0000 1101 0	1	0	37	0	13	1	0	4	1	0	0	0	0
2	10 0100101	000 1101 00	1	0	37	0	13	1	0	4	2	0	1	0	0
3	10 1 001011	0000 1101 0	1	2	11	0	13	1	1	4	1	0	1	0	0
4	10 10 01011	00000 1101	1	2	11	0	13	1	2	4	0	1	0	0	0
5	10 1 001011	0000 1101 0	1	2	11	0	13	1	1	4	1	1	0	0	0
6	10 0001011	000 1101 01	1	0	11	2	13	1	0	4	2	1	1	0	1
7	10 0001011	1000 1101 0	1	0	11	2	13	1	0	4	1	1	1	0	0
8	010 001101	10000 1011	2	0	13	1	11	2	0	4	0	0	0	1	0
9	010 001101	0000 1011 1	2	0	13	1	11	2	0	4	1	0	1	1	0
10	010 1 00010	10000 1011	2	1	2	1	11	2	1	4	0	1	0	1	0
11	010 000010	1000 1011 1	2	0	2	3	11	2	0	4	1	1	1	1	1
12	110 001011	0100000 10	3	0	11	2	2	2	0	2	0	0	0	0	0
13	110 001011	100000 10 0	3	0	11	2	2	2	0	2	1	0	0	0	0
14	110 001011	00000 10 01	3	0	11	2	2	2	0	2	2	0	0	0	0
15	110 001011	0000 10 010	3	0	11	2	2	2	0	2	3	0	1	0	0
16	110 1 00011	00000 10 01	3	4	3	2	2	2	1	2	2	0	1	0	0
17	110 10 0011	100000 10 0	3	4	3	2	2	2	2	2	1	0	1	0	0
18	110 101 001	0100000 10	3	5	1	2	2	2	3	2	0	1	0	0	0
19	110 10 0001	010000 10 1	3	4	1	5	2	2	2	2	1	1	0	0	0
20	110 1 00001	10000 10 10	3	4	1	5	2	2	1	2	2	1	0	0	0
21	110 000001	0100 10 100	3	0	1	17	2	2	0	2	3	1	1	0	1
22	110 000001	00100 10 10	3	0	1	17	2	2	0	2	2	1	1	0	0
23	110 000001	000100 10 1	3	0	1	17	2	2	0	2	1	1	1	0	0
24	100010 010	11000000 1	17	0	2	3	1	5	0	1	0	0	0	1	0
25	100010 010	1000000 1 1	17	0	2	3	1	5	0	1	1	0	0	1	0
26	100010 010	000000 1 11	17	0	2	3	1	5	0	1	2	0	1	1	0
27	100010 1 00	1000000 1 1	17	2	0	3	1	5	1	1	1	0	1	1	0
28	100010 10 0	11000000 1	17	2	0	3	1	5	2	1	0	1	0	1	0
29	100010 1 00	1000000 1 1	17	2	0	3	1	5	1	1	1	1	0	1	0
30	100010 000	100100 1 10	17	0	0	37	1	5	0	1	2	1	1	1	1
31	100010 000	0100100 1 1	17	0	0	37	1	5	0	1	1	1	1	1	0
32	Terminated	Terminated	37	0	1	17	0	6	0	0	0	0	0	0	0
33	Terminated	Terminated	37	0	1	17	0	6	0	0	1	0	0	0	0
34	Terminated	Terminated	37	0	1	17	0	6	0	0	2	0	0	0	0
35	Terminated	Terminated	37	0	1	17	0	6	0	0	3	0	0	0	0
36	Terminated	Terminated	37	0	1	17	0	6	0	0	4	0	0	0	0

Table 4: An execution example of our space-efficient EEA for $p = 37$ and $x = 13$. The table mainly illustrates how the two $(n + 3)$ -qubit registers **Work1** and **Work2** are allocated during the execution to store the variables t, q, r and t', r' , respectively.

Removing redundant arithmetic and shift operations. In the baseline version, several arithmetic and shift operations between different phases are functionally redundant. Specifically, we have:

- In phases 1 and 2: comparison, addition, subtraction between $(r, 2^{\ell_s} r')$;
- In phases 3 and 4: comparison, addition, subtraction between $(t', 2^{\ell_s} t)$;
- In phases 1 and 3: a one-position left shift on `Work2`;
- In phases 2 and 4: a one-position right shift on `Work2`.

By combining the control conditions of these operations (or equivalently, the corresponding quantum control wires), we can eliminate redundant operations from the circuit. This optimization results in a total of two groups of location-controlled addition/subtraction operations and two location-controlled swaps in one step. Here, *location-control* refers to arithmetic operations applied conditionally on specific positions of the two `Work` registers, with the active positions indicated by the `Length` registers.

Merging location-controlled swaps. To further decrease the circuit depth and gate count, we observe that the two location-controlled swaps appearing in phases 2 and 3 act on the same qubit position of `Work1`. We merge them into a single swap controlled by $\text{Phase1} \oplus \text{Phase2}$. The required update of ℓ_q depends on the phase: ℓ_q is increased in phase 2 and decreased in phase 3.

Algorithm pseudocode and overall complexity. After applying the above optimizations, the overall asymptotic quantum resource estimation per step is summarized as follows:

- Five location-controlled arithmetic operations, including one swap, two additions, and two subtractions; along with four length updates at the termination step of an EEA iteration. Each of these operations costs $O(n)$ gates in the implementation presented in Section 4.
- Four position shifts and one $(n + 3)$ -qubit SWAP, each requiring $O(n)$ quantum gates.

With these optimizations, one step of our space-efficient EEA proceeds as in Algorithm 3.

4 Quantum Circuit Implementation of Modular Inversion

In this section, we present the explicit quantum circuit implementation of a single step of the space-efficient EEA with register sharing, as described in Algorithm 3. Throughout the section, we use the same quantum register notation as in the algorithm.

The full circuit construction is, however, too complex to be depicted within a small number of circuit diagrams. This difficulty is mainly due to the presence of location-controlled arithmetic operations, which are highly non-standard. To present the construction in a relatively more explicit manner, we first describe the overall circuit structure in Section 4.1, where the location-controlled arithmetic operations are treated as circuit blocks; we then provide a detailed implementation of these operations in Section 4.4. In all circuit diagrams, the black triangle denotes the output wire that carries the result of the corresponding circuit block; and we denote $\ell = \lfloor \log_2 n \rfloor$ for convenience.

Algorithm 3 Optimized one step of our EEA implementation

Require: Work1 register stores $|t, q, r\rangle$, Work2 register stores $|t', r'\rangle$;

Require: Length registers store $|\ell_t, \ell_q, \ell_{r'}, \ell_s\rangle$;

Require: Control registers store $|\text{Phase1}, \text{Phase2}, \text{Iter}, \text{Sign}\rangle$.

```
if Phase1 = 0 then ▷ Pre-shift operations
    Perform a one-position left shift on Work2, and update  $\ell_s \leftarrow \ell_s + 1$ 
    if Phase2 = 1 then
        Perform a two-position right shift on Work2, and update  $\ell_s \leftarrow \ell_s - 2$ 
    end if
     $(\text{Sign}, r) \leftarrow (\text{Sign}, r) - 2^{\ell_s} r'$  ▷ Arithmetic block 1: location-controlled subtraction on  $r$ 's
    if Phase2 = 1 then
         $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
    end if
    if Phase2 = 0 or Sign = 0 then
         $r \leftarrow r + 2^{\ell_s} r'$ 
    end if
end if
if Phase1  $\oplus$  Phase2 = 1 then ▷ Arithmetic block 2: location-controlled swap
    Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1
    if Phase1 = 1 then
         $\ell_q \leftarrow \ell_q - 1$ 
    else
         $\ell_q \leftarrow \ell_q + 1$ 
    end if
end if
if Phase1 = 1 then ▷ Arithmetic block 3: location-controlled addition on  $t$ 's
    if Phase2 = 1 or Sign = 0 then
         $t' \leftarrow t' - 2^{\ell_s} t$ 
    end if
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
     $(\text{Sign}, t') \leftarrow (\text{Sign}, t') + 2^{\ell_s} t$ 
    Perform a one-position left shift on Work2, and update  $\ell_s \leftarrow \ell_s + 1$  ▷ Post-shift operations
    if Phase2 = 1 then
        Perform a two-position right shift on Work2, and update  $\ell_s \leftarrow \ell_s - 2$ 
    end if
end if
if  $\ell_q = 0$  and  $\ell_{r'} > 0$  then ▷ Phase update logic;  $\ell_{r'} = 0$  indicates algorithm termination
     $\text{Phase2} \leftarrow \text{Phase2} \oplus \text{Sign} \oplus \text{Phase1}$ ,  $\text{Sign} \leftarrow \text{Sign} \oplus \text{Phase2}$ 
end if
if  $\ell_s = 0$  then
     $\text{Phase1} \leftarrow \text{Phase1} \oplus 1$ ,  $\text{Phase2} \leftarrow \text{Phase2} \oplus 1$ 
end if
if  $\ell_q = 0$  and  $\ell_s = 0$  then ▷ Register swapping at the end of one EEA iteration
    Swap Work1 and Work2
    Update  $\ell_t$  to the bit length of the new  $t$ ,  $\ell_{r'}$  to the bit length of the new  $r'$ 
     $\text{Iter} \leftarrow \text{Iter} \oplus 1$ 
end if
```

4.1 Overall circuit implementation of one step

According to Algorithm 3, the overall circuit implementation of a single iteration of our space-efficient EEA is shown in Figures 5 and 6, presented in a continuous layout. Both circuit diagrams are divided into several algorithmic components, indicated by dashed boxes. Each component corresponds exactly to one arithmetic block specified in Algorithm 3.

In both circuit diagrams, **Shift** denotes a position shift of the workspace: a positive value represents a left shift, while a negative value represents a right shift. The circuit blocks **Add**, **Sub**, and **Swap** denote location-controlled addition, subtraction, and swap operations, respectively. At the end of each EEA iteration, the circuit block labeled **SWAP** represents a full SWAP operation applied to all qubits in the registers **Work1** and **Work2**; this block is distinct from the **Swap** block to avoid ambiguity. Finally, the **Len** block denotes the update operations on the length registers.

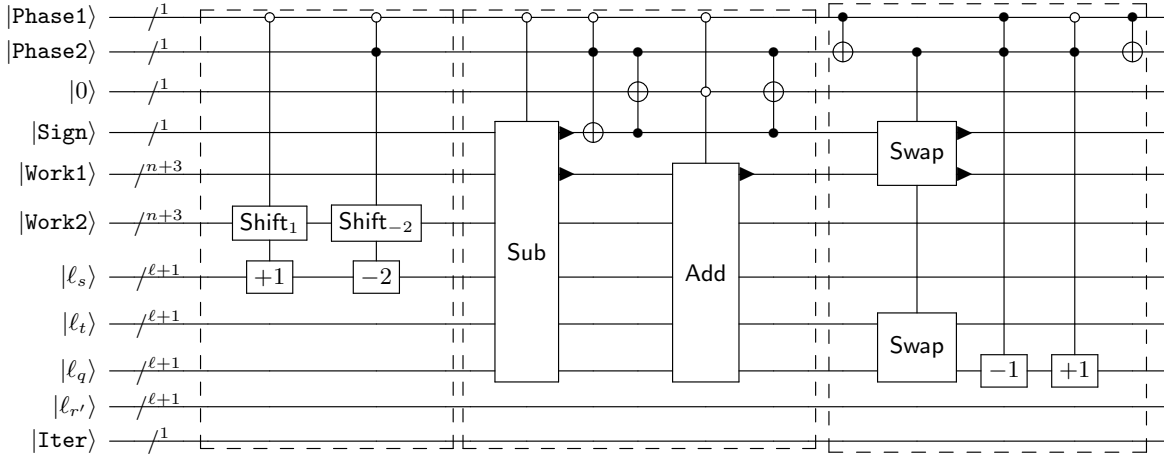


Figure 5: Overall circuit implementation (first half) of a single iteration of our space-efficient EEA. The three dashed boxes, from left to right, represent: (1) pre-shift operations; (2) location-controlled subtraction on r 's; (3) location-controlled swap.

4.2 Step-dependent active windows

To reduce the quantum gate complexity for implementing our space-efficient EEA, we introduce step-dependent active windows for each location-controlled operation. As illustrated in the figures of the previous subsection, we define k and K as known bounds on the active indices of the **Work** registers.

For instance, at step T , a location-controlled Swap circuit acts on the $(\ell_t + \ell_q + 1)$ -th qubit of the **Work1** register. Over all possible inputs x used to compute the modular inverse $x^{-1} \bmod p$, the quantity $\ell_t + \ell_q + 1$ is bounded below by $k := k(T)$ and above by $K := K(T)$. Therefore, applying location-controlled operations to qubits in the **Work1** register with indices outside the interval $[k, K]$ is unnecessary. We refer to this interval as the *active window*.

We next specify the step-dependent active windows for each type of location-controlled operation. All bounds are taken over all *possible inputs* x , namely, those inputs x for which the location-controlled

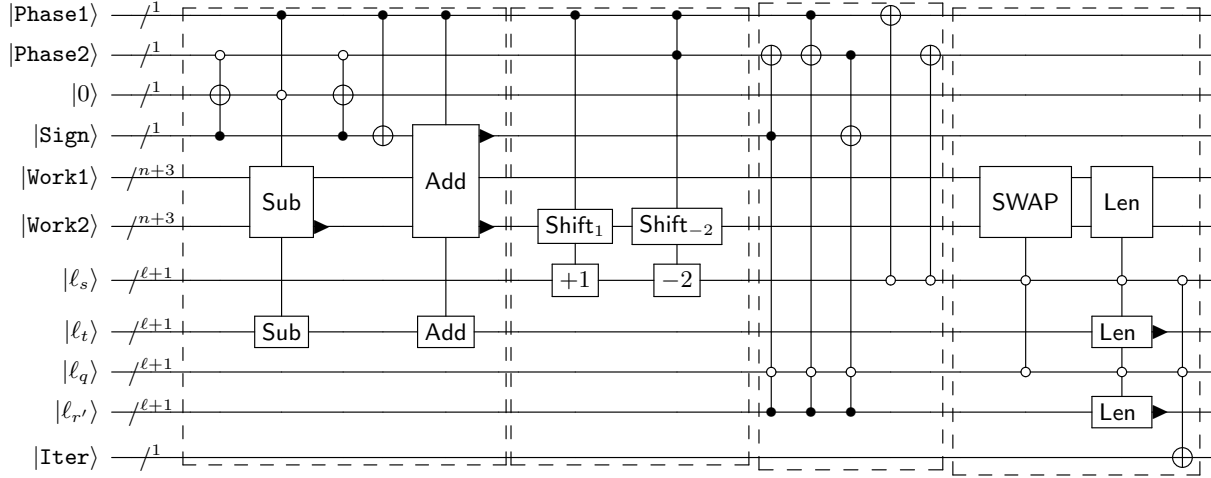


Figure 6: Overall circuit implementation (second half) of a single iteration of our space-efficient EEA, continued from Figure 5. The four dashed boxes, from left to right, represent: (1) location-controlled addition on t 's; (2) post-shift operations; (3) phase update; (4) swapping Work1 and Work2 , together with the corresponding length updates at the end of one EEA iteration.

circuits are activated by the outer control qubits. The constant c equals to $1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$. We defer the proofs to Appendix A.2.

- **Location-controlled addition/subtraction on r 's.** These operations act on qubits indexed from $(\ell_t + \ell_q + 2)$ to $(n + 3 - \ell_s)$. The upper bound $K_1 = K_1(T) = n + 3$; the lower bound $k_1 = k_1(T)$ is defined by

$$\ell_t + \ell_q + 2 \geq k_1(T) := \max \left\{ \left\lceil \frac{T - n - 2}{4c - 1} \right\rceil, 1 \right\} + 2.$$

- **Location-controlled swap.** These operations act on the $(\ell_t + \ell_q + 1)$ -th qubit. The two-sided bounds are defined by

$$\begin{aligned} \ell_t + \ell_q + 1 &\geq k_2(T) := \max \left\{ \left\lceil \frac{T - 3(n + 2)}{4c - 3} \right\rceil, 1 \right\} + 1, \\ \ell_t + \ell_q + 1 &\leq K_2(T) := \min \{ \lfloor T/2 \rfloor + 2, n + 2 \}. \end{aligned}$$

- **Location-controlled addition/subtraction on t 's.** These operations act on the first $(\ell_t + 1)$ qubits. This is a one-sided controlled operation, the upper bound $K_3(T)$ is defined by

$$\ell_t + 1 \leq K_3(T) := \min \{ \lceil T/4 \rceil + 1, n + 1 \}.$$

- **Length-update circuit for updating ℓ_t .** We execute the length-update circuit only at step indices T that are multiples of four. This circuit acts on qubits indexed from ℓ_t to $(n + 3 - \ell_{r'})$, and the corresponding two-sided active window is defined by

$$\begin{aligned} \ell_t &\geq k_4(T) := \max \left\{ \left\lceil \frac{T - 4(n + 2)}{4c - 4} \right\rceil, 1 \right\}, \\ n + 3 - \ell_{r'} &\leq K_4(T) := \min \{ T/4 + 3, n + 3 \}. \end{aligned}$$

- **Length-update circuit for updating $\ell_{r'}$.** Let $\ell_t^*, \ell_{r'}^*$ denote the updated value of $\ell_t, \ell_{r'}$ after the length update. This circuit acts on qubits indexed from $\ell_t^* + 2$ to $(n + 4 - \ell_{r'}^*)$, and the corresponding two-sided active window is defined by

$$\ell_t^* + 2 \geq k_5(T) := \lceil T/(4c) \rceil,$$

$$n + 4 - \ell_{r'}^* \leq K_5(T) := \min \{T/4 + 4, n + 3\}.$$

4.3 Unary iteration

We will use unary iteration [BBG⁺18] to implement location-controlled operations on a known interval of the two **Work** registers. Let **L** be a **Length** register promised to store a value $a \in \{k, k + 1, \dots, K\}$, let **W** be a **Work** register, and let c be an optional external control qubit. The operation has the form

$$\mathcal{U}_{[k,K]} = |0\rangle\langle 0|_c \otimes I + |1\rangle\langle 1|_c \otimes \sum_{j=k}^K |j\rangle\langle j|_{\mathbf{L}} \otimes U_j,$$

where U_j is a unitary operation on **W** selected by the value j . Equivalently, the operation performs $|c\rangle|a\rangle|\psi\rangle \mapsto |c\rangle|a\rangle U_a^c |\psi\rangle$ for all $a \in [k, K]$.

The main primitive used by unary iteration is a reversible AND. The compute and uncompute forms of this gate are shown in Figure 7. In the Toffoli/CNOT counting convention used here, computing an AND costs one Toffoli gate, while uncomputing an AND using measurement costs one CNOT gate with no Toffoli gates.

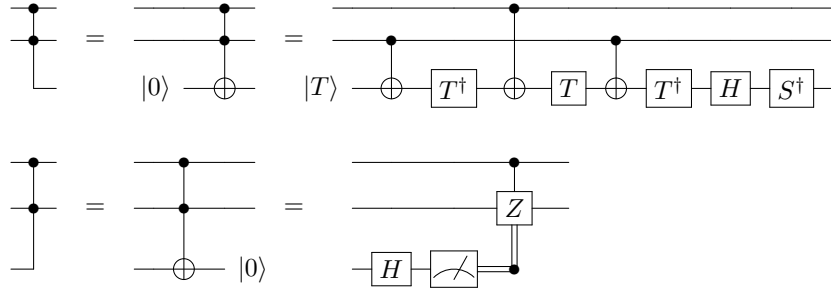


Figure 7: Compute and uncompute forms of the reversible AND primitive, reproduced from [BBG⁺18].

For a general interval, unary iteration can be viewed as a binary tree whose leaves are the labels $k, k + 1, \dots, K$. Each internal node stores a subset of labels. If the current node has control bit g , we choose the most significant bit position b that is not constant on its labels, thereby separating them into two nonempty subsets according to the value of A_b . For an increasing-order traversal, we first compute $h = g(1 - A_b)$ with one reversible AND, use h as the control for the $A_b = 0$ child, then switch the same temporary bit by a CNOT, $h \leftarrow h \oplus g$, so that $h = gA_b$ controls the $A_b = 1$ child. After the second child is processed, h is uncomputed. At a leaf j , the current control bit is exactly

$$e_j = c[a = j],$$

and the circuit applies U_j controlled on e_j . For a decreasing-order traversal, the two children are visited in the opposite order. Figure 8 illustrates this construction for the interval $\{5, 6, 7, 8\}$.

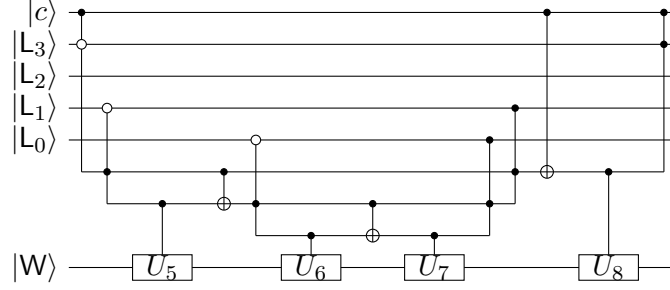


Figure 8: Pruned unary iteration on the promised interval $A \in \{5, 6, 7, 8\}$. The labels are split by the bits of A only when the split separates the remaining candidates. The temporary control is reused to visit the two children of each split, and the leaves apply U_5, U_6, U_7, U_8 in increasing order.

If $M = K - k + 1$, the tree has M leaves and $M - 1$ internal nodes. Thus the selection logic contributes $M - 1 = K - k$ Toffoli gates, while the leaf operations contribute the cost of the controlled U_j gates themselves. For $M \geq 2$, the recursion depth, and hence the number of temporary control qubits, is at most $\lceil \log_2(M - 1) \rceil + 1$. For the trivial case $M = 1$, no temporary control qubit is needed. This replaces independent equality tests for all j , which would cost $O(M \log_2 n)$ Toffoli gates for an $O(\log_2 n)$ -bit index register, by a linear-size selection circuit using only $O(\log_2 M)$ temporary control qubits.

4.4 Location-controlled operations

In this subsection, the two **Work** registers are indexed, from left to right, by $u_1, u_2, \dots, u_{n+3}$ and $v_1, v_2, \dots, v_{n+3}$, respectively.

Location-controlled Swap circuit. We first consider the location-controlled swap operation appearing in Figure 5. The goal is to swap the **Sign** qubit with the $(\ell_t + \ell_q + 1)$ -th qubit of **Work1**, while the whole operation is controlled by an external qubit **Ctrl**. Let $J = \ell_t + \ell_q + 1$, where k and K are known constants such that $k \leq J \leq K$. After temporarily storing J in the ℓ_q register, the location-controlled swap can be written as

$$\text{Swap}_{[k, K]} = |0\rangle\langle 0|_{\text{Ctrl}} \otimes I + |1\rangle\langle 1|_{\text{Ctrl}} \otimes \sum_{j=k}^K |j\rangle\langle j|_{\ell_q} \otimes \text{SWAP}(\text{Sign}, u_j),$$

where the subscript ℓ_q denotes the temporary register storing J .

This operation can be implemented directly using unary iteration. We first reversibly transform the ℓ_q register as $|\ell_t\rangle|\ell_q\rangle \mapsto |\ell_t\rangle|\ell_t + \ell_q + 1\rangle$. Using **Ctrl** as the global control, pruned unary iteration over the labels $k, k + 1, \dots, K$ then produces, one value at a time, the control bit $e_j = \text{Ctrl} \wedge [J = j]$. When this unary control is active, we swap **Sign** and u_j . After it finishes we restore the ℓ_q register to its original value. Figure 9 illustrates this construction for the example $k = 5$ and $K = 8$.

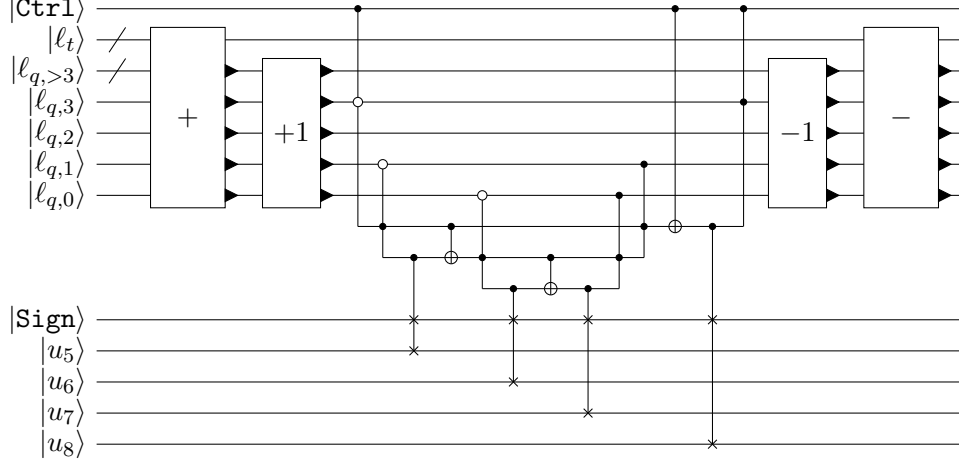


Figure 9: Location-controlled swap circuit for $k = 5$ and $K = 8$. After computing $J = \ell_t + \ell_q + 1$, pruned unary iteration over the labels 5, 6, 7, 8 selects the work qubit to be swapped with **Sign**.

The unary iterator contributes $K - k + O(1)$ Toffoli gates and $2(K - k) + O(1)$ CNOT gates, the controlled swaps contribute $K - k + O(1)$ Toffoli gates and $2(K - k) + O(1)$ CNOT gates. The reversible transformations of the ℓ_q register contribute $O(\log_2 n)$ Toffoli/CNOT gates. Thus the location-controlled Swap circuit uses $2(K - k) + O(\log_2 n)$ Toffoli gates and $4(K - k) + O(\log_2 n)$ CNOT gates.

Location-controlled Add, Sub circuit. We next describe the location-controlled addition and subtraction circuits. As a representative example, consider the operation

$$(\mathbf{Sign}, r) \leftarrow (\mathbf{Sign}, r) - 2^{\ell_s} r', \quad (3)$$

where **Sign** records the sign of the subtraction result. In terms of physical positions in the two **Work** registers, this operation acts only on the interval

$$L = \ell_t + \ell_q + 2, \quad R = n + 3 - \ell_s.$$

That is, the relevant qubits are $u_L, \dots, u_R$ in **Work1** and $v_L, \dots, v_R$ in **Work2**; outside this interval all qubits are left unchanged. The shift by ℓ_s is already reflected in the endpoint $R = n + 3 - \ell_s$, so the aligned bits $v_L, \dots, v_R$ represent the contribution of $2^{\ell_s} r'$ to the subtraction. For a known active window $[k, K]$, we promise that $k \leq L \leq R \leq K$.

If the endpoints L and R were fixed, the subtraction could be implemented by a ripple-carry subtractor on the qubit pairs (u_j, v_j) for $j \in [L, R]$ with a dedicated carry qubit c initialized to $|0\rangle$. For the subtraction in Equation (3), we first apply the $\mathbf{UMA}^\dagger$ cells from high to low, update **Sign** from the carry qubit, and then apply the $\mathbf{MAJ}^\dagger$ cells from low to high to uncompute the carry.

It remains to coherently select the interval $[L, R]$. The endpoint registers storing L and R are obtained from the length registers by reversible affine transformations, which are undone after the arithmetic block. The circuit uses one accumulator bit s , initialized to $|0\rangle$. In the $\mathbf{UMA}^\dagger$ pass, the circuit scans the physical

positions from high to low, namely $j = K, K - 1, \dots, k$. For each scanned position j , pruned unary iteration on the endpoint registers coherently produces the two local controls

$$\lambda_j = \text{Ctrl} \wedge [R = j], \quad \mu_j = \text{Ctrl} \wedge [L = j].$$

The circuit first updates the accumulator by $s \leftarrow s \oplus \lambda_j$. If the updated value of s is 1, the circuit applies $\text{UMA}^\dagger(c, u_j, v_j)$; otherwise it does nothing on (c, u_j, v_j) . After this controlled arithmetic cell, the circuit updates the accumulator by $s \leftarrow s \oplus \mu_j$. Therefore, when the scan reaches $j = R$, the bit λ_j flips s from 0 to 1 before the arithmetic cell, so the $\text{UMA}^\dagger$ cell at $j = R$ is applied. For positions strictly inside the interval, the accumulator remains equal to 1, so the corresponding arithmetic cells are also applied. When the scan reaches $j = L$, the $\text{UMA}^\dagger$ cell is still applied, and then μ_j flips s back to 0. The same update rule is used for every scanned position $j \in [k, K]$. Before the active interval is reached, all arithmetic cells are disabled, so the carry qubit c remains equal to 0 at the interval entrance.

After the $\text{UMA}^\dagger$ pass, c stores the carry bit of the selected subtraction. We update **Sign** by

$$\text{Sign} \leftarrow \text{Sign} \oplus c.$$

The $\text{MAJ}^\dagger$ pass visits $j = k, k + 1, \dots, K$. At each position, the accumulator is first updated by $s \leftarrow s \oplus \mu_j$. If the updated value of s is 1, the circuit applies $\text{MAJ}^\dagger(c, u_j, v_j)$. It then updates the accumulator by $s \leftarrow s \oplus \lambda_j$. Therefore the $\text{MAJ}^\dagger$ cells are applied exactly for $j \in [L, R]$, and s and c are restored to $|0\rangle$ at the end.

Figure 10 illustrates the complete pattern for the example $k = 5$ and $K = 7$.

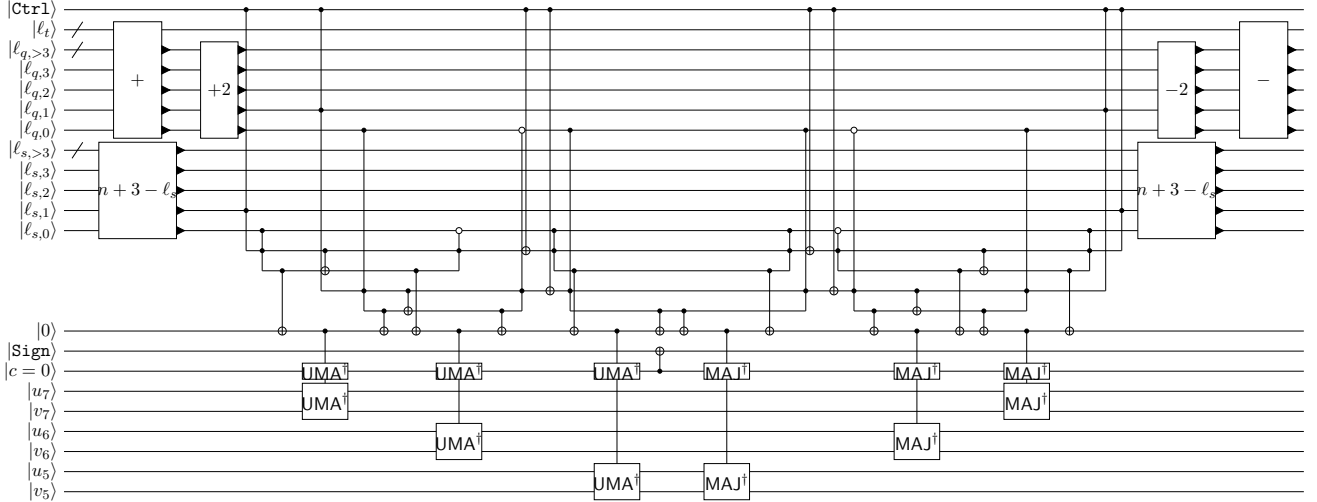


Figure 10: Location-controlled subtraction circuit for $k = 5$ and $K = 7$. The $\text{UMA}^\dagger$ pass computes the carry, **Sign** is updated from c , and the $\text{MAJ}^\dagger$ pass restores the carry qubit.

Finally, we explain how the controlled MAJ and UMA cells used above are implemented. We do not add the location-control bit to every gate in the cell; only the Toffoli gate that updates the carry qubit is controlled. Figure 11 shows the corresponding controlled cells.

The gate count consists of the following contributions:



Figure 11: Controlled arithmetic cells used in the location-controlled add/sub circuits.

- Generating $[L = j]$ and $[R = j]$ during both scans requires four applications of unary iteration. They use $4(K - k) + O(1)$ Toffoli gates and $8(K - k) + O(1)$ CNOT gates in total.
- Applying one controlled $\text{UMA}^\dagger$ cell at each position in the high-to-low scan uses $4(K - k) + O(1)$ Toffoli gates and $2(K - k) + O(1)$ CNOT gates.
- Applying one controlled $\text{MAJ}^\dagger$ cell at each position in the low-to-high scan uses $3(K - k) + O(1)$ Toffoli gates and $2(K - k) + O(1)$ CNOT gates.
- Computing L and R from ℓ_q and ℓ_s , and subsequently restoring these registers, uses $O(\log_2 n)$ Toffoli and CNOT gates.

Adding these terms, the location-controlled **Sub** circuit implementing Equation (3) uses $11(K - k) + O(\log_2 n)$ Toffoli gates and $12(K - k) + O(\log_2 n)$ CNOT gates.

Location-controlled length-update circuit. Finally, we describe the length-update circuit. We focus on updating ℓ_t ; the circuit for updating $\ell_{r'}$ is analogous. At the end of one EEA iteration, after the full swap of **Work1** and **Work2**, the left part of **Work1** stores the current value of t , while the left part of **Work2** stores the current value of t' . Let $L_{\text{new}} = \text{len}(t)$, $L_{\text{old}} = \text{len}(t')$. Since the value stored in ℓ_t before the update is L_{old} , it suffices to implement

$$\ell_t \leftarrow \ell_t \oplus L_{\text{old}} \oplus L_{\text{new}}.$$

Thus the length update is reduced to two serial constant-XOR writes: first XOR the old length, and then XOR the new length.

We first describe the subroutine for XORing L_{new} into ℓ_t . This subroutine finds the highest valid nonzero position among the qubits $u_k, \dots, u_K$. Only positions in the left region not occupied by r' should be inspected. Let $J = n + 3 - \ell_{r'}$ be the right boundary of this valid region with the promise $k \leq \ell_t \leq J \leq K$ from the active window under consideration. For each $j \in [k, K]$, define the masked bit

$$a_j = \text{Ctrl} \wedge [j \leq J] \wedge u_j.$$

Also define bits

$$z_j = \bigwedge_{h=j}^K \neg a_h.$$

Thus $z_j = 1$ means that no valid nonzero bit occurs among positions $j, j+1, \dots, K$. If the highest valid nonzero position is m , then

$$z_K = \dots = z_{m+1} = 1, \quad z_m = \dots = z_k = 0.$$

If no valid nonzero bit exists in the window, then all z_j are equal to 1.

The highest position can be written using a telescoping XOR. We first XOR the classical constant K into the length register. Then, for $j = K, K-1, \dots, k+1$, whenever $z_j = 1$, we change the current candidate from j to $j-1$ by XORing the classical constant $j \oplus (j-1)$. Finally, if $z_k = 1$, then the entire window contains no valid nonzero bit, and we clear the remaining candidate k by XORing k . Equivalently, the value written by the subroutine is

$$L_{\text{new}} = K \oplus \bigoplus_{j=k+1}^K z_j \cdot (j \oplus (j-1)) \oplus z_k \cdot k,$$

where a term such as $z_j \cdot C$ means that the classical bit string C is XORed into the length register controlled on z_j . If the highest valid nonzero position is m , the expression telescopes to m . If no such position exists, it telescopes to zero.

It remains to implement the constant writes controlled by the bits z_j without storing all of them in clean ancillae. Borrow dirty qubits $g_k, \dots, g_K$, which will be restored at the end. For $j > k$, let V_j denote the Clifford operation that XORs the classical constant $j \oplus (j-1)$ into the length register, and let V_k denote the operation that XORs k . Since each V_j is a product of CNOT gates, $V_j^2 = I$. Assume for the moment that we can perform the transformation

$$g_j \leftarrow g_j \oplus z_j \quad (j = k, \dots, K).$$

Then the desired controlled write is implemented by placing this transformation between two uses of V_j controlled by the borrowed qubit:

$$V_j^{g_j}, \quad g_j \leftarrow g_j \oplus z_j, \quad V_j^{g_j}.$$

Indeed, if the initial value of the borrowed qubit is G_j , then the two controlled writes are

$$V_j^{G_j} V_j^{G_j \oplus z_j} = V_j^{z_j},$$

so the unknown initial value cancels. After all constant writes are completed, we perform the same transformation again to restore every g_j to its original value. Figure 12 illustrates this method for the example $k = 5$ and $K = 7$.

We now explain how to implement the transformation $g_j \leftarrow g_j \oplus z_j$ for all j . The recurrence is

$$z_K = \neg a_K, \quad z_j = \neg a_j z_{j+1} \quad (j < K).$$

To implement this transformation, first apply, for $j = k, k+1, \dots, K-1$, the Toffoli gates $g_j \leftarrow g_j \oplus (\neg a_j)g_{j+1}$. Then apply the base CNOT gate $g_K \leftarrow g_K \oplus \neg a_K$. Finally apply the same Toffoli gates in

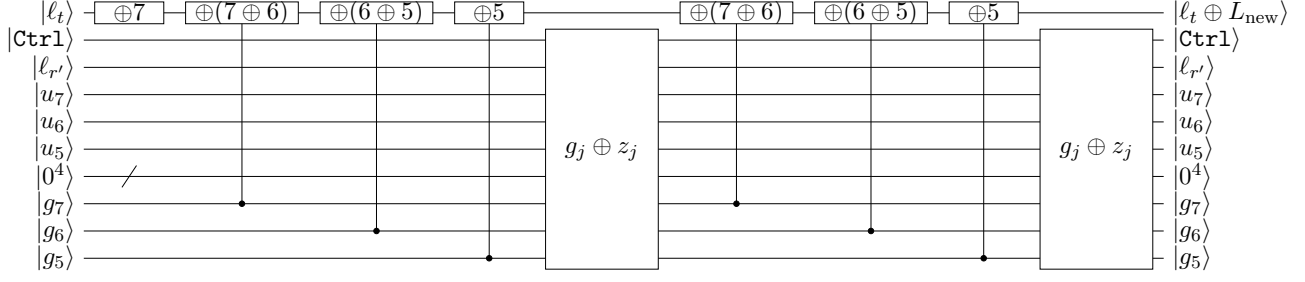


Figure 12: Writing L_{new} using borrowed qubits for $k = 5$ and $K = 7$. The boxes labeled $g_j \oplus z_j$ denote the transformation $g_j \leftarrow g_j \oplus z_j$ for all j in the window.

reverse order, for $j = K - 1, K - 2, \dots, k$. For a fixed $j < K$, the two Toffoli gates acting on g_j are separated by the transformation $g_{j+1} \leftarrow g_{j+1} \oplus z_{j+1}$. Therefore their combined action on g_j is

$$\begin{aligned} g_j &\leftarrow g_j \oplus (\neg a_j)g_{j+1} \oplus (\neg a_j)(g_{j+1} \oplus z_{j+1}) \\ &= g_j \oplus (\neg a_j)z_{j+1} = g_j \oplus z_j. \end{aligned}$$

The bit a_j is produced only locally when the corresponding gate is applied. During a scan of the window, unary iteration on the boundary register supplies the temporary range control

$$b_j = \text{Ctrl} \wedge [j \leq J].$$

The circuit then computes $a_j = b_j \wedge u_j$ into one clean temporary qubit, uses it as the negative control in the corresponding Toffoli or CNOT, and immediately uncomputes it. The required range controls are supplied by one scan in the order $k, k + 1, \dots, K$ and one scan in the reverse order $K, K - 1, \dots, k$.

Figure 13 shows this transformation for the example $k = 5$ and $K = 7$. The boundary value is computed in place on the $\ell_{r'}$ register, and the temporary bit a is created only when the corresponding update gate is applied.

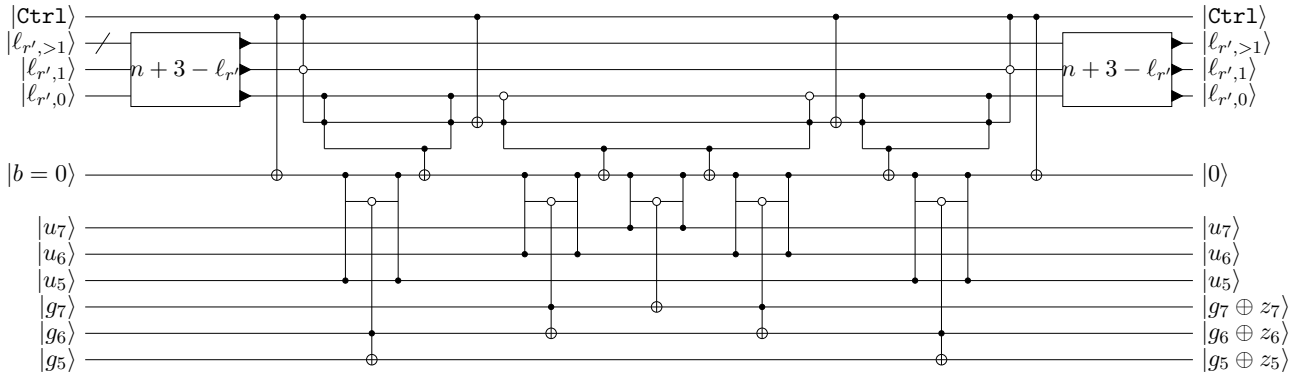


Figure 13: Computing $g_j \leftarrow g_j \oplus z_j$ for $k = 5$ and $K = 7$.

To update ℓ_t , we invoke this subroutine twice. First we use the analogous construction with v_j in place of u_j and borrow the qubits u_j as the dirty register g_j , which XORs L_{old} into ℓ_t . Then we use the

construction described above and borrow the qubits v_j as the dirty register g_j , which XORs L_{new} into ℓ_t . The two calls are serial, and the borrowed dirty qubits are restored after each call.

We now give the explicit resource count. First consider one application of $g_j \leftarrow g_j \oplus z_j$ for all $j \in [k, K]$. Its gate count has three contributions:

- The forward and reverse unary iterations use $2(K - k) + O(1)$ Toffoli gates and $4(K - k) + O(1)$ CNOT gates.
- The forward and reverse applications of $g_j \leftarrow g_j \oplus (\neg a_j)g_{j+1}$ contribute $2(K - k)$ Toffoli gates in total, while the update at $j = K$ contributes one CNOT gate.
- The temporary bit $a_j = b_j \wedge u_j$ is computed once in each direction and uncomputed immediately after use. Over both directions, this uses $2(K - k) + O(1)$ Toffoli gates and $2(K - k) + O(1)$ CNOT gates.

Thus one application of $g_j \leftarrow g_j \oplus z_j$ uses $6(K - k) + O(\log_2 n)$ Toffoli gates and $6(K - k) + O(\log_2 n)$ CNOT gates.

To XOR either L_{old} or L_{new} into ℓ_t , the transformation $g_j \leftarrow g_j \oplus z_j$ is first applied between the two sets of controlled constant XORs and is then applied again to restore the qubits g_j . These two applications use $12(K - k) + O(\log_2 n)$ Toffoli gates and $12(K - k) + O(\log_2 n)$ CNOT gates. Each set of controlled constant XORs uses $2(K - k) + O(\log_2 n)$ CNOT gates and no Toffoli gates. Therefore, XORing one of the two lengths into ℓ_t uses $12(K - k) + O(\log_2 n)$ Toffoli gates and $16(K - k) + O(\log_2 n)$ CNOT gates.

The complete length update performs this procedure once for L_{old} and once for L_{new} . Its total cost is $24(K - k) + O(\log_2 n)$ Toffoli gates and $32(K - k) + O(\log_2 n)$ CNOT gates.

The construction uses exactly $K - k + 1$ dirty auxiliary qubits, all of which are restored to their initial states. The same clean auxiliary qubits can be reused throughout the circuit: one stores a_j , one stores b_j , and unary iteration requires at most $\lceil \log_2(K - k) \rceil + 1$ additional clean qubits for $K - k \geq 1$. Thus the construction uses at most $\lceil \log_2(K - k) \rceil + 3$ clean auxiliary qubits.

5 Affine Point Addition with Mid-Circuit Measurement

In the previous sections, we constructed a space-efficient modular inversion circuit based on the extended Euclidean algorithm. The inversion circuit uses two n -qubit field registers together with $O(\log_2 n)$ auxiliary qubits. In this section, we explain how to incorporate this component into an affine point-addition circuit. By allowing mid-circuit measurements and classical feed-forward operations, the affine point-addition block can be implemented using only three n -qubit field registers, plus the $O(\log_2 n)$ auxiliary qubits required by the EEA inversion subroutine.

The overall circuit is shown in Figure 14. The three main quantum registers are denoted by X , Y , and A , each storing an element of $\mathbb{F}_p$. The remaining $O(\log_2 n)$ EEA ancilla qubits are not shown explicitly in the figure.

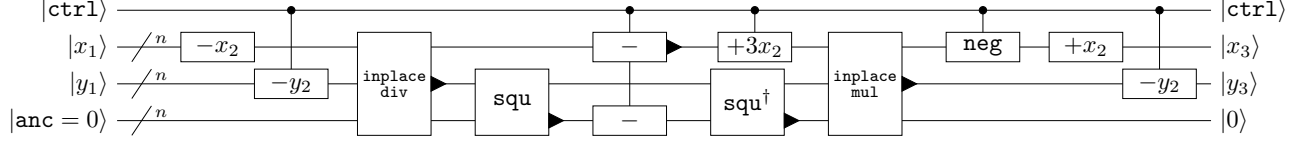


Figure 14: Affine point-addition circuit with mid-circuit measurements using three n -qubit field registers.

The constant additions, subtractions, negations, and squarings in Figure 14 are standard in-place modular operations. The only non-standard components are the in-place division and multiplication subroutines. They have the following abstract interfaces:

$$\text{IDiv} : |x\rangle_X |y\rangle_Y |0\rangle_A \mapsto |x\rangle_X |y/x\rangle_Y |0\rangle_A, \quad x \neq 0, \quad (4)$$

$$\text{IMul} : |x\rangle_X |y\rangle_Y |0\rangle_A \mapsto |x\rangle_X |xy\rangle_Y |0\rangle_A, \quad x \neq 0. \quad (5)$$

It remains to explain how the in-place maps in Equations (4) and (5) can be implemented with only three field registers. The constructions are similar, so we describe the in-place division subroutine in detail. Let S denote the $O(\log_2 n)$ auxiliary register used by the EEA inversion circuit. The goal is to implement

$$|x\rangle_X |y\rangle_Y |0\rangle_A |0\rangle_S \mapsto |x\rangle_X |y/x\rangle_Y |0\rangle_A |0\rangle_S, \quad x \neq 0.$$

First, run the forward EEA inversion circuit on X , using A as the large clean workspace and S as the small auxiliary register:

$$|x\rangle_X |y\rangle_Y |0\rangle_A |0\rangle_S \mapsto |x^{-1}\rangle_X |y\rangle_Y |0\rangle_A |\Gamma(x)\rangle_S.$$

Here $|\Gamma(x)\rangle_S$ denotes the intermediate EEA state that is kept until the inverse EEA circuit is applied. Next, use a standard modular multiplication to write the quotient into A :

$$|x^{-1}\rangle_X |y\rangle_Y |0\rangle_A \mapsto |x^{-1}\rangle_X |y\rangle_Y |y/x\rangle_A.$$

At this point A is no longer clean, and therefore cannot be used as the large workspace for the inverse EEA circuit. Instead, we recycle the register Y by measurement. Apply $H^{\otimes n}$ to Y and measure it in the computational basis. If the classical outcome is $b \in \{0, 1\}^n$, the remaining quantum state acquires the phase $(-1)^{b \cdot y}$, where the dot product is over $\mathbb{F}_2$. The measured register Y is then reset to $|0\rangle$.

Now Y is a clean n -qubit register, so it can be used as the large workspace for the inverse EEA circuit. Applying the inverse EEA circuit gives

$$(-1)^{b \cdot y} |x^{-1}\rangle_X |0\rangle_Y |y/x\rangle_A |\Gamma(x)\rangle_S \mapsto (-1)^{b \cdot y} |x\rangle_X |0\rangle_Y |y/x\rangle_A |0\rangle_S. \quad (6)$$

The phase in Equation (6) is removed by recomputing the measured value y from x and y/x . Specifically, apply the modular multiplication

$$|x\rangle_X |0\rangle_Y |y/x\rangle_A \mapsto |x\rangle_X |y\rangle_Y |y/x\rangle_A, \quad (7)$$

then apply the classically controlled Pauli correction

$$Z^b = Z^{b_0} \otimes Z^{b_1} \otimes \dots \otimes Z^{b_{n-1}}$$

to the register Y . This contributes another factor $(-1)^{b \cdot y}$ and therefore cancels the measurement phase. Finally, reverse the multiplication in Equation (7), obtaining

$$|x\rangle_X |0\rangle_Y |y/x\rangle_A.$$

Swapping Y and A completes the in-place division:

$$|x\rangle_X |y/x\rangle_Y |0\rangle_A.$$

The corresponding circuit is shown in Figure 15.

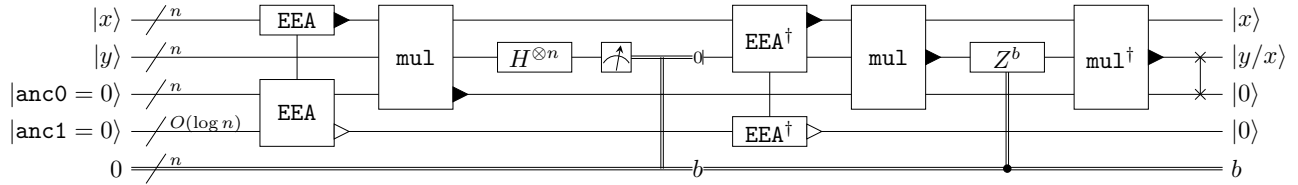


Figure 15: In-place division with mid-circuit measurement and classical feed-forward operations.

The in-place multiplication subroutine is implemented by the same mechanism. One first computes xy into the clean register A , measures and resets the old $Y = y$ register, uses the remaining registers to recompute y for the Z^b phase correction, uncomputes this recomputation, and finally swaps Y with A . Thus both IDiv and IMul require only the three field registers X, Y, A , together with the $O(\log_2 n)$ EEA auxiliary register S . Therefore the affine point-addition circuit in Figure 14 uses $3n + O(\log_2 n)$ logical qubits.

6 Resource Estimation and the ECDLP

We adopt the resource-estimation methodology introduced by Roetteler et al. [RNSL17]. In Shor’s algorithm for the ECDLP, the dominant quantum cost arises from the sequence of controlled elliptic-curve point additions performed in superposition. We consider the point additions in affine coordinates over the finite field $\mathbb{F}_p$, where p is an n -bit prime. At this level, point addition reduces to a fixed sequence of modular additions, subtractions, multiplications, squarings, and inversions. Among these operations, modular inversion typically dominates both the space complexity and the Toffoli gate count.

6.1 Space complexity improvements

In this work, we focus exclusively on reducing the space complexity required for modular inversion, rather than exploring trade-offs among Toffoli count, circuit depth, and space complexity as previous works [RNSL17, HJN⁺20, BZG⁺26, Sch26]. Specifically, we present an exact, space-efficient, in-place

reversible quantum circuit for modular inversion that implements Equation (1). The circuit is based on the register-sharing technique originally proposed by Proos and Zalka [PZ03]. This approach reduces the number of qubits required for modular inversion to

$$2n + 6 \lfloor \log_2 n \rfloor + 19.$$

Of this total, $2n + 4 \lfloor \log_2 n \rfloor + 15$ qubits correspond to the base circuit shown in Figures 5 and 6, while the remaining $2 \lfloor \log_2 n \rfloor + 4$ qubits are required for the unary iteration described in Section 4.3.

For elliptic curve point addition shown in Figure 14, the overall space complexity is then

$$3n + 6 \lfloor \log_2 n \rfloor + 19.$$

6.2 Asymptotic gate counts

Modular inversion. We first derive the asymptotic Toffoli and CNOT gate counts of the proposed modular inversion circuit. Since the circuit consists of several types of location-controlled operations, we first recall (in Section 4.4) the gate cost incurred by each circuit block at algorithmic step T . These per-step costs are summarized in Table 5. We then combine them with the active-window analysis developed in Section 4.2 to obtain the overall asymptotic gate complexity.

Circuit block on step T	Toffoli cost	CNOT cost
Location-controlled addition/subtraction on r 's	$11(K_1(T) - k_1(T))$	$12(K_1(T) - k_1(T))$
Location-controlled swap	$2(K_2(T) - k_2(T))$	$4(K_2(T) - k_2(T))$
Location-controlled addition/subtraction on t 's	$9(K_3(T) - k_3(T))$	$10(K_3(T) - k_3(T))$
Length-update circuit for ℓ_t (only on $4 T$)	$24(K_4(T) - k_4(T))$	$32(K_4(T) - k_4(T))$
Length-update circuit for $\ell_{r'}$ (only on $4 T$)	$24(K_5(T) - k_5(T))$	$32(K_5(T) - k_5(T))$

Table 5: Per-step Toffoli and CNOT gate counts of the major circuit blocks in the modular inversion algorithm.

- **Location-controlled addition/subtraction on r 's.** These operations cost

$$2 \sum_{T=1}^{4\lceil cn \rceil} 11(K_1(T) - k_1(T)) + O(n \log_2 n) = (44c + 11)n^2 + O(n \log_2 n)$$

Toffoli gates, and $(48c + 12)n^2 + O(n \log_2 n)$ CNOT gates.

- **Location-controlled swap.** These operations cost

$$\sum_{T=1}^{4\lceil cn \rceil} 2(K_2(T) - k_2(T)) + O(n \log_2 n) = (4c + 1)n^2 + O(n \log_2 n)$$

Toffoli gates, and $(8c + 2)n^2 + O(n \log_2 n)$ CNOT gates.

- **Location-controlled addition/subtraction on t 's.** These operations cost

$$2 \sum_{T=1}^{4\lceil cn \rceil} 9(K_3(T) - k_3(T)) + O(n \log_2 n) = (72c - 36)n^2 + O(n \log_2 n)$$

Toffoli gates, and $(80c - 40)n^2 + O(n \log_2 n)$ CNOT gates.

- **Length-update circuit for updating ℓ_t .** We execute the length-update circuit only at step indices T that are multiples of four. These operations cost

$$\sum_{T'=1}^{\lceil cn \rceil} 24(K_4(4T') - k_4(4T')) + O(n \log_2 n) = 12cn^2 + O(n \log_2 n).$$

Toffoli gates, and $16cn^2 + O(n \log_2 n)$ CNOT gates.

- **Length-update circuit for updating $\ell_{r'}$.** We execute the length-update circuit only at step indices T that are multiples of four. These operations cost

$$\sum_{T'=1}^{\lceil cn \rceil} 24(K_4(4T') - k_4(4T')) + O(n \log_2 n) = (12c - 12)n^2 + O(n \log_2 n).$$

Toffoli gates, and $(16c - 16)n^2 + O(n \log_2 n)$ CNOT gates.

In addition to the circuit blocks analyzed above, the modular inversion circuit (illustrated in Figures 5 and 6) contains four controlled Shift circuits. Each Shift circuit consists of $n + O(1)$ Toffoli gates and $2n + O(1)$ CNOT gates. Therefore, these four Shift circuits contribute an additional $16cn^2 + O(n)$ Toffoli gates and $32cn^2 + O(n)$ CNOT gates.

Combining all contributions, the total number of Toffoli gates required by our (one-sided without reversion) modular inversion circuit grows asymptotically as

$$(160c - 36)n^2 + O(n \log_2 n) \approx 194.47n^2 + O(n \log_2 n).$$

The asymptotic bound of CNOT gates required is

$$(200c - 42)n^2 + O(n \log_2 n) \approx 246.09n^2 + O(n \log_2 n).$$

Point addition. As discussed in Section 5, we count one affine point addition with mid-circuit measurement as consisting of 1 in-place division, 1 in-place multiplication, 2 modular squarings, and a constant number of modular additions/subtractions/negations. The corresponding circuit is shown schematically in Figure 14. Among these modular arithmetic operations, the modular additions/subtractions/negations contribute only $O(n \log_2 n)$ Toffoli gates in total and are therefore absorbed into the lower-order term. The in-place division, as well as the in-place multiplication, consists of 2 modular divisions and 3 modular multiplications as shown in Figure 15.

We use an improved modular multiplication/squaring circuit described in Appendix B, which costs $17n^2 + O(n \log_2 n)$ Toffoli gates. Therefore, a single affine point addition with mid-circuit measurement can be implemented by at most

$$(4 \cdot 194.47 + 6 \cdot 17 + 2 \cdot 17)n^2 + O(n \log_2 n) < 914n^2 + O(n \log_2 n)$$

Toffoli gates.

6.3 Numerical experiments

All resource-estimation experiments were conducted on a Linux server equipped with an AMD EPYC 7302 processor (up to 3.0 GHz). Circuit generation, compilation and optimization were performed using IBM Qiskit. The constructed circuits were transpiled into a gate basis consisting of CCX, CX, and X gates, in order to obtain accurate Toffoli-gate and CNOT-gate counts.

The implementation follows the explicit circuit constructions in Sections 4 and 5. Since modular inversion is the most involved subroutine and a main contributor to the point-addition cost, we report its implementation separately.

- **Modular-inversion subroutine.** We implement the one-step EEA circuit as a collection of Qiskit modules. These modules include the pre-shift and post-shift blocks, the location-controlled arithmetic and swap blocks, the phase-update logic, and the length-update circuits. A full inversion instance is generated by following the step schedule of Algorithm 3. Each step instantiates only its active window. The step circuits are counted in chunks and are then combined with the shared-register EEA wrapper.
- **Point-addition circuit.** We implement the point-addition circuit blockwise. Figure 14 specifies the top level affine point addition schedule, including the constant coordinate updates, the in-place division and multiplication calls, the square-minus block, and the final corrections. The point coordinates x_2 and y_2 are treated as classically precomputed constants. The in-place division and multiplication blocks are assembled according to Figure 15, from the shared-register EEA circuit, modular multiplication blocks, inverse multiplication blocks, and the explicit mid-circuit measurements and feed-forward phase corrections shown in the figure.

To obtain the compiled gate counts of these implemented circuits, we use a layered blockwise counting pipeline. This is necessary because directly expanding the full point-addition circuit into a single Qiskit circuit over elementary operations is impractical. We first recursively decompose and count reusable Qiskit subblocks, including constant-coordinate updates, controlled modular additions and subtractions, modular doubling and halving, and the shared-register EEA wrapper. We then assemble larger arithmetic blocks from these counted components with their exact multiplicities. For example, a modular multiplication block contains n controlled modular additions and $n - 1$ modular doublings, while its inverse contains n controlled modular subtractions and $n - 1$ modular halvings. The squaring block reuses the same multiplication count and adds the explicit CNOT cost for copy and uncompute. This yields a complete compiled gate count for the point-addition circuit while preserving the block multiplicities.

In addition to compiling and counting the reusable subblocks, we apply a local template-based optimization before each subblock count is stored and reused. The optimizer performs local cancellation and Qiskit template replacement on small reversible segments. To make the template identities directly applicable, we restrict these segments to the gate library $\{X, CX, CCX\}$. A rewritten segment is accepted only if its gate count does not increase.

To improve efficiency and preserve the circuit structure, we apply the optimization segment by segment. We scan each decomposed subblock linearly and collect consecutive X , CX , and CCX gates into one reversible segment. When the scan reaches any other instruction, the current segment is optimized, the out-of-library instruction is counted directly, and a new segment is started. Thus, in circuits with measurements and feed-forward phase corrections, these operations are not rewritten. They simply separate the neighboring reversible segments. If a segment exceeds the runtime limits, it is counted unchanged.

To validate the implementation, we developed test suites for both the modular-inversion and point-addition circuits. The tests include representative examples over prime fields with p ranging from small values such as $p = 3$ to 512-bit primes, and with circuit widths n ranging up to 512. They additionally verify register layouts, circuit schedules, arithmetic sub-blocks, and compiled block assembly.

The corresponding circuit implementation is included in our open-source codebase.² For each problem size n , we generated the full circuit instance up to the theoretical upper bound on the number of cycles derived in this work, transpiled it into the CCX , CX , and X basis, and recorded the resulting gate counts. We report results for $n \in \{64, 128, 160, 192, 224, 256, 384, 512\}$. The numerical values are listed in Table 6.

n	Modular inversion		Point addition	
	Toffoli ($\times 10^6$)	CNOT ($\times 10^6$)	Toffoli ($\times 10^6$)	CNOT ($\times 10^6$)
64	1.91	2.97	4.21	6.89
128	6.70	10.51	14.97	24.81
160	10.05	15.89	22.56	37.68
192	14.12	22.36	31.78	53.21
224	18.88	29.93	42.58	71.40
256	24.66	38.96	58.78	99.30
384	53.45	84.92	128.15	219.77
512	93.96	149.10	225.69	388.63

Table 6: Gate counts for modular inversion and point addition circuits over n -bit prime fields.

6.4 Resource estimates for Shor’s ECDLP circuit

For the full ECDLP attack, we do not repeat the controlled point-addition circuit bit-by-bit for all $2n$ control bits. Instead, we follow the signed-window technique of [HJN⁺20, Section 5.1]. Namely, we partition the $2n$ control bits arising in the double-scalar multiplication into windows of size w , and implement each window by one signed windowed point addition.

²GitHub repository: <https://github.com/ZeroWang030221/Space-Efficient-Quantum-Algorithm-for-Elliptic-Curve-Discrete-Logarithms-with-Resource-Estimation>

In the signed-window construction, one of the w bits is used as a sign bit, while the remaining $w - 1$ bits address a precomputed table of point multiples. As shown schematically in Fig. 10 of [HJN⁺20], one such windowed point addition uses the arithmetic core of an affine Weierstrass point addition. The coordinates of the selected precomputed point are obtained through three table queries, and its sign is handled by one modular negation. In our space-optimized circuit, these three queries are implemented by five sequential table look-ups.³ Since the dominant n^2 term in our Toffoli accounting comes from modular divisions, multiplications and squaring, replacing the classically known addend by an addend obtained from the look-up table does not change the asymptotic scaling.

To obtain a clean asymptotic bound, we choose window size $w = 2 \log_2 n$. The five sequential table look-ups contribute $5 \cdot 2^w$ Toffoli gates to each windowed point addition. The full double-scalar multiplication uses approximately $2n/w$ windows, so its dominant Toffoli count becomes

$$\frac{2n}{w} (914n^2 + 5 \cdot 2^w + O(n \log_2 n)) = 919 \frac{n^3}{\log_2 n} + O(n^2).$$

For $n = 256$, following the analysis in [BZG⁺26], the Toffoli count of the complete Shor ECDLP circuit is estimated as

$$28 \cdot (5 \cdot 2^{16} + Q_A). \quad (8)$$

Here, Q_A denotes the Toffoli count of a single controlled affine point-addition circuit. For a window size of $w = 16$, the number of signed-window point additions is $\frac{2n}{w} - 4 = 28$. The five sequential table look-ups described above incur an additional $5 \cdot 2^w$ Toffoli gates per window, which becomes $5 \cdot 2^{16}$ when $w = 16$. Substituting our concrete value of $Q_A(256)$ shows that our algorithm requires $2^{30.63}$ Toffoli gates for the curve secp256k1.

Finally, we note that compression techniques and multi-run tradeoffs [Eke19] could potentially yield further improvements to the constant factors in our overall resource estimates.

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³The circuit first queries (x_2, y_2) , then x_2 , and finally (x_2, y_2) . If two free n -qubit registers were available, the two coordinates in each (x_2, y_2) query could be loaded together. Since only one free n -qubit register is available in our space-optimized circuit, each (x_2, y_2) query is split into two sequential look-ups, giving $2 + 1 + 2 = 5$ look-ups in total.

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A Proof Details

A.1 Bounds on the total number of steps

Suppose that after k iterations of the Extended Euclidean Algorithm, we obtain $r_{k-1} = 1$ and $r_k = 0$, with intermediate quotients $q_1, q_2, \dots, q_{k-1}$, where $q_i = \lfloor r_{i-1}/r_i \rfloor$ for $i = 1, 2, \dots, k-1$. Then the total number of steps required in our four-phase algorithm can be expressed as

$$N = 4 \sum_{i=1}^{k-1} (\lfloor \log_2 q_i \rfloor + 1).$$

The lower bound of N can be derived directly. Since $r_{i-1} = q_i r_i + r_{i+1} < (q_i + 1)r_i$, it follows that

$$N \geq 4 \sum_{i=1}^{k-1} \log_2(q_i + 1) > 4 \sum_{i=1}^{k-1} \log_2 \frac{r_{i-1}}{r_i} = 4 \log_2 p \geq 4(n-1).$$

Because N must be a multiple of 4, we conclude that $N \geq 4n$.

To derive the upper bound of N , we take a complementary viewpoint. Instead of fixing p and computing N , we fix N and seek the smallest possible value of p as k and the quotient sequence $\{q_i\}_{i=1}^{k-1}$ vary. Note that $p = r_0$ can be reconstructed recursively from the sequence defined by $r_k = 0$, $r_{k-1} = 1$, and $r_{i-1} = r_{i+1} + q_i r_i$, $i = k-1, k-2, \dots, 1$. To minimize p under this recurrence, we apply the following sequence of adjustment steps, keeping $N = 4 \sum_{i=1}^{k-1} (b_i + 1)$ fixed:

- We first adjust all quotients to powers of two, i.e., $q_i = 2^{b_i}$ with $b_i = \lfloor \log_2 q_i \rfloor$. This modification is justified because reducing any quotient strictly decreases the corresponding sequence $r_{i-1}, \dots, r_0$.
- For any $i = 1, 2, \dots, k-2$, if $b_i \geq 2$ for $i = 1$ and $b_i \geq 1$ for $i > 1$, we can split the EEA iteration with quotient $q_i = 2^{b_i}$ into two successive iterations with quotients $q_{i,1} = 1$ and $q_{i,2} = 2^{b_i-1}$. The updated value of r_{i-1} is then

$$r'_{i-1} = r_i + q_{i,1}(r_{i+1} + q_{i,2}r_i) = r_{i+1} + (2^{b_i-1} + 1)r_i \leq r_{i+1} + 2^{b_i}r_i = r_{i-1},$$

implying that the modified sequence yields a smaller p . The condition $b_1 \geq 2$ when $i = 1$ is required since the algorithm assumes $x < p/2$.

- If $b_{k-1} \geq 2$, we further refine the final iteration with $q_{k-1} = 2^{b_{k-1}}$ by splitting it into two iterations with quotients $q_{k-1,1} = 2$ and $q_{k-1,2} = 2^{b_{k-1}-2}$. This adjustment differs from the previous one because r_{k-2} must remain greater than 1. The updated value of r_{k-2} becomes

$$r'_{k-2} = 1 + q_{k-1,1} \cdot q_{k-1,2} = 1 + 2^{b_{k-1}-1} < 2^{b_{k-1}} = r_{k-2},$$

showing once again that the adjustment leads to a smaller p for the same total number of steps.

After applying all possible adjustments, we obtain a quotient sequence of form $\{q_i\} = \{2, 1, 1, \dots, 1, 2\}$ with length $k-1 = N/4 - 2$. The corresponding sequence of r_i satisfies

$$r_{k-1} = 1, \quad r_{k-2} = 2, \quad r_{i-1} = r_{i+1} + r_i \text{ for } i = k-2, \dots, 2, \quad \text{and } r_0 = r_2 + 2r_1.$$

This recurrence defines a Fibonacci sequence with $r_{k-i} = F_{i+1}$ for $i = 1, 2, \dots, k-1$, and the minimal possible value of p is thus $p = r_0 = F_{k-1} + 2F_k = F_{k+2} = F_{N/4+1}$. Together with the condition $2^{n-1} \leq p < 2^n$, we obtain

$$\frac{1}{\sqrt{5}} \left(\frac{\sqrt{5}+1}{2} \right)^{N/4+1} \leq F_{N/4+1} + 1 \leq p + 1 \leq 2^n.$$

Hence,

$$N \leq 4 \left\lfloor c \left(n + \log_2 \sqrt{5} \right) - 1 \right\rfloor \leq 4 \lceil cn \rceil,$$

where $c = 1/\log_2 \left(\frac{\sqrt{5}+1}{2} \right)$.

A.2 Step-dependent active windows

Fix an input x , let $(q_1, \dots, q_{k-1})$ denote the quotient sequence produced by EEA, and define $b_i := \lfloor \log_2 q_i \rfloor$ for each iteration i . Under the four-phase schedule, each EEA iteration i is expanded into $4(b_i + 1)$ steps. The total number of steps is $N = 4 \sum_{i=1}^{k-1} (b_i + 1) \leq N_{\max} := 4 \lceil cn \rceil$, where $c = 1/\log_2 \left(\frac{\sqrt{5}+1}{2} \right)$ (see Appendix A.1).

For a global step index $T \in \{1, 2, \dots, N_{\max}\}$, let $j = j(x, T)$ denote the index of the EEA iteration that contains step T , and let $u = u(x, T)$ denote the position of T within that iteration. More precisely, the pair $(j(x, T), u(x, T))$ is uniquely determined by the conditions

$$\sum_{i=1}^{j-1} 4(b_i + 1) < T \leq \sum_{i=1}^j 4(b_i + 1), \quad u = T - \sum_{i=1}^{j-1} 4(b_i + 1).$$

The bit-length of the current quotient $\ell_q(x, T)$ depends deterministically on indices (j, u) :

$$\ell_q(x, T) = \begin{cases} 0 & u(x, T) \in (0, b_j + 1] \cup (3(b_j + 1), 4(b_j + 1)], \\ u(x, T) - (b_j + 1) & u(x, T) \in (b_j + 1, 2(b_j + 1)], \\ 3(b_j + 1) - u & u(x, T) \in (2(b_j + 1), 3(b_j + 1)]. \end{cases} \quad (9)$$

We next state a lemma that characterizes the minimal possible value of t_j , conditioned on the total number of steps N_j taken before reaching the j -th iteration of EEA. The proof follows exactly the same adjustment argument as in Appendix A.1, and is therefore omitted.

Lemma A.1. *Suppose that $N_j = \sum_{i=1}^{j-1} 4(b_i + 1)$ is fixed. Then, over all possible EEA iteration indices j and all admissible quotient sequences $(q_1, \dots, q_{j-1})$, we have $t_j \geq F_{N_j/4+1}$, and consequently,*

$$\lfloor \log_2 t_j \rfloor + 1 \geq \log_2 \left(\frac{\sqrt{5}+1}{2} \right) \cdot \frac{N_j}{4}.$$

Here, $\{F_k\}_{k \geq 0}$ denotes the Fibonacci sequence $F_0 = 0, F_1 = 1$, and $F_{k+2} = F_{k+1} + F_k$ for all $k \geq 0$.

We then provide the detailed proofs of the bounds stated in Section 4.2 in the remainder of this subsection. Recall that $c = 1/\log_2 \left(\frac{\sqrt{5}+1}{2} \right)$.

Location-controlled addition/subtraction on r 's. First, observe that $t_j q_j < t_{j+1} < p$, which implies $\ell_t + b_j \leq n + 1$. Since a location-controlled addition/subtraction on r 's is only activated in Phase 1 and 2, i.e. $0 < u \leq 2(b_j + 1)$, we then analyze the claimed bound by considering two cases.

- **Case 1.** Suppose that $u \leq b_j + 1$. In this case, we have $\ell_q = 0$. By Lemma A.1, it follows that

$$\ell_t \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - (n + 2 - \ell_t)}{4},$$

$$\text{hence } \ell_t + \ell_q = \ell_t \geq \frac{T - n - 2}{4c - 1}.$$

- **Case 2.** Suppose that $b_j + 1 < u \leq 2(b_j + 1)$. Then $\ell_q = u - (b_j + 1)$, and we obtain that

$$\ell_t + \ell_q \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} + (u - b_j - 1).$$

The right-hand side is minimized when $u = b_j + 1$, in which case the expression reduces to that of Case 1.

Combining the two cases, we conclude that $\ell_t + \ell_q + 2 \geq \max \left\{ \left\lceil \frac{T - n - 2}{4c - 1} \right\rceil, 1 \right\} + 2$.

Location-controlled swaps. For the lower bound, a location-controlled swap is only activated in Phase 2 and 3, i.e. $b_j + 1 < u \leq 3(b_j + 1)$, we then analyze the claimed lower bound by considering two cases.

- **Case 1.** Suppose that $b_j + 1 < u \leq 2(b_j + 1)$. In this case, we also have $\ell_t + \ell_q \geq \frac{T - n - 2}{4c - 1}$.
- **Case 2.** Suppose that $2(b_j + 1) < u \leq 3(b_j + 1)$. In this case, we have $\ell_q = 3(b_j + 1) - u$. By Lemma A.1, it follows that

$$\ell_t \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - 3(n + 2 - \ell_t)}{4},$$

$$\text{hence } \ell_t + \ell_q \geq \ell_t \geq \frac{T - 3(n + 2)}{4c - 3}.$$

Combining the two cases, we conclude that $\ell_t + \ell_q + 1 \geq \max \left\{ \left\lceil \frac{T - 3(n + 2)}{4c - 3} \right\rceil, 1 \right\} + 1$.

For the upper bound, recall the recurrence relation of the EEA on the t -sequence, that is $t_{i+1} = t_{i-1} + q_i t_i < (q_i + 1)t_i \leq 2^{b_i+1} t_i$. By iterating this inequality, we obtain that

$$t = t_j \leq \prod_{i=1}^{j-1} 2^{b_i+1} = 2^{(T-u)/4}, \quad \text{and then } \ell_t \leq (T - u)/4 + 1.$$

By Equation (9), we know that $\ell_q \leq u/2$. Hence,

$$\ell_t + \ell_q + 1 \leq \lfloor (T - u)/4 + u/2 + 2 \rfloor = \lfloor (T + u)/4 \rfloor + 2 \leq \lfloor T/2 \rfloor + 2.$$

Finally, since the **Work1** register stores a value $r \geq 1$, we conclude that $\ell_t + \ell_q + 1 \leq n + 2$.

Location-controlled addition/subtraction on t 's. As shown above, we have that $\ell_t + 1 \leq \lfloor (T - u)/4 \rfloor + 2 \leq \lceil T/4 \rceil + 1$. Under the constraint that $t \leq p < 2^n$, we also obtain that $\ell_t + 1 \leq n + 1$.

Length-update circuit. For the lower bound $k_4(T)$, the length-update circuit is activated only at the end of an EEA iteration, namely when $u = 4(b_j + 1)$. By Lemma A.1, we have

$$\ell_t \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - 4(n + 2 - \ell_t)}{4},$$

which implies $\ell_t \geq \frac{T - 4(n + 2)}{4c - 4}$.

For the lower bound $k_5(T)$, Lemma A.1 directly yields

$$\ell_t^* \geq \log_2 \left(\frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T}{4} = \frac{T}{4c}.$$

For the upper bound $K_5(T)$, recall the recurrence relation of the EEA on the r -sequence, $r_{i-1} = r_{i+1} + q_i r_i < (q_i + 1)r_i \leq 2^{b_i+1} r_i$. By iterating this inequality, we obtain

$$p/r_{j+1} \leq \prod_{i=1}^j 2^{b_i+1} = 2^{T/4}.$$

It follows that $n + 4 - \ell_{r'}^* < n + 4 - \log_2 r_{j+1} \leq T/4 + n + 4 - \log_2 p \leq T/4 + 5$, and hence $n + 4 - \ell_{r'}^* \leq T/4 + 4$.

For the upper bound $K_4(T)$, we similarly have $n + 3 - \ell_{r'} \leq n + 3 - \ell_{r'}^* \leq T/4 + 3$.

B Improved Modular Multiplication Circuit

Our modular multiplier used in in-place division/multiplication implements

$$\text{Mul}_p : |x\rangle|y\rangle|0\rangle \mapsto |x\rangle|y\rangle|xy \bmod p\rangle,$$

based on the usual Horner double-and-add scan as the low-space multiplier of [RNSL17]. The circuit contains n controlled modular additions and $n - 1$ modular doublings.

- **Controlled modular additions.** The controlled modular addition

$$|c\rangle|A\rangle|B\rangle|0\rangle_f \mapsto |c\rangle|A\rangle|B + cA \bmod p\rangle|0\rangle_f,$$

is implemented by first doing the controlled addition $B \leftarrow B + cA \pmod{2^n}$, while XORing the overflow carry into a flag f . We use a specialized controlled quantum–quantum ripple-carry adder for this step, rather than controlling every gate of an ordinary adder from [CDKM04]. Let γ_i denote the carry into bit i , with $\gamma_0 = 0$, and $\gamma_{i+1} = \text{maj}(A_i, B_i, \gamma_i)$.

During the forward sweep, the circuit computes the carry chain. At bit i , the addend and accumulator wires are temporarily transformed to $A_i \oplus \gamma_i$ and $B_i \oplus \gamma_i$, while the carry wire is advanced

to γ_{i+1} . In the reverse sweep, we first undo the carry Toffoli, so the carry wire again contains γ_i . A CNOT from this carry wire to the accumulator wire restores $B_i \oplus \gamma_i \mapsto B_i$. At this point the addend wire still contains $A_i \oplus \gamma_i$. We then apply the controlled sum-writing Toffoli

$$\text{CCX}(c, A_i \oplus \gamma_i; B_i).$$

Thus, if $c = 0$, the accumulator bit remains B_i ; if $c = 1$, it becomes $B_i \oplus A_i \oplus \gamma_i$, which is exactly the i -th sum bit. Finally, a CNOT from the carry wire to the addend wire restores $A_i \oplus \gamma_i \mapsto A_i$. Therefore, the controlled writing of the n sum bits contributes precisely n additional Toffoli gates. In addition, after the forward sweep the final carry γ_n is copied into the overflow flag only when $c = 1$, using one more CCX gate,

$$f \leftarrow f \oplus c\gamma_n.$$

Hence this controlled variant of ripple-carry adder costs $3n + O(1)$ Toffoli gates.

Let $S = B + cA$, then after the first step the accumulator contains

$$\tilde{B} = S \bmod 2^n,$$

and the overflow bit

$$h = \lfloor S/2^n \rfloor$$

has been XORed into the flag. Since $A, B_{\text{old}} < p < 2^n$, we have $S \leq 2p - 2 < 2^{n+1}$, so $h \in \{0, 1\}$. The true reduction condition is $S \geq p$. If $h = 0$, then $\tilde{B} = S$, so this condition is exactly $[\tilde{B} \geq p]$. If $h = 1$, then reduction is certainly needed, while $\tilde{B} = S - 2^n < p$, so $[\tilde{B} \geq p] = 0$. Hence the reduction bit is

$$r = h \oplus [\tilde{B} \geq p].$$

We therefore update the flag by XORing in the fixed-modulus comparison $[\tilde{B} \geq p]$, which is evaluated by the classical-quantum comparator from [Gid25]. Here we use the dirty-assisted adder which costs $3n + O(1)$ Toffoli gates by borrowing the non-target register A as dirty workspace. Controlled on this flag, we subtract the fixed modulus p from B , again using the same Gidney-style controlled classical-quantum subtractor, with cost $3n + O(1)$. Finally, after the correction, the flag can be uncomputed by one Toffoli gate applying

$$f \leftarrow f \oplus c[B_{\text{final}} < A].$$

$[B_{\text{final}} < A]$ can be evaluated using the high-bit-only Cuccaro quantum comparator, derived from the Cuccaro ripple-carry adder [CDKM04], costing $2n + O(1)$ Toffoli gates. All clean and borrowed dirty workspace, including the flag f , is restored at the end of the block.

Therefore, one controlled modular addition costs

$$T_{\text{add}}(n) = (3n + O(1)) + (3n + O(1)) + (3n + O(1)) + (2n + O(1)) = 11n + O(1)$$

Toffoli gates.

- **Modular doublings.** For modular doubling, we follow the implementation from [RNSL17]. The binary doubling itself is implemented by Clifford shift/CNOT operations. Since p is odd, the reduction flag can be cleared from the least significant output bit. The only parts that require Toffoli gates are one fixed comparison with p and one conditional fixed subtraction, which can be implemented by the same classical-quantum adder from [Gid25].

Therefore, one modular doubling costs

$$T_{\text{dbl}}(n) = (3n + O(1)) + (3n + O(1)) = 6n + O(1)$$

Toffoli gates.

Consequently, the total number of Toffoli gates required by our modular multiplication circuit grows asymptotically as

$$T(n) = nT_{\text{add}}(n) + (n - 1)T_{\text{dbl}}(n) = 17n^2 + O(n).$$

The modular squaring circuit is same to the modular multiplication, but with the addend equal to the input register itself. Therefore, it also costs at most $17n^2 + O(n)$ Toffoli gates.