

Factoring 2048 bit RSA integers with a half-million-qubit modular atomic processor

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Shor's algorithm is one of the most promising applications of quantum computers. However, since $\sim 10^6$ physical qubits are believed to be required for established approaches, the algorithm will need to be distributed across many modules. In this paper, we provide a distributed compilation of Shor's algorithm on a modular atomic processor. We present an end-to-end compilation and optimization strategy that focuses on the interplay between the inter-module communication and the intra-module clock rate. With a half-million-qubit modular atomic processor with a communication rate of 10^5 Bell pairs per second and a measurement time of 1 ms in a CPU-inspired architecture, we demonstrate that 2048-bit RSA integers can be factored in only 16% more time than a single-module architecture. Our work presents the first end-to-end analysis and simulation of large-scale integer factorization on modular atomic hardware and it provides a blueprint for the future design of other large-scale modular algorithms.

I. INTRODUCTION

Shor's algorithm is one of the few quantum algorithms with a promised quantum advantage, where the time complexity of factoring n -bit integers is reduced from $O(e^n)$ to $O(\text{poly}(n))$ [1–14]. This potential utility combined with its highly specific goal make it a unique benchmark for designing processor architectures and for resource requirement estimation. The estimated physical qubit count required for RSA 2048 has decreased from $\sim 10^9$ in 2010 to $\sim 10^6$ in 2025 [2, 3, 7, 8, 12–14]. This decrease was largely fueled by advances in magic state cultivation, windowed quantum arithmetic, and the replacement of long modular exponential with short discrete logarithms [2, 4, 15]. These rapid developments bring Shor's algorithm to the near future, and in this paper, we will present an end-to-end compilation of Shor's algorithm on the neutral atom hardware platform.

In the past several months, further reductions have been proposed, based on quantum error correction codes such as the quantum low density parity check (qLDPC) codes that have a much higher encoding rate than traditional CSS codes such as the surface code or Steane code [16, 17]. The high-rate code can further reduce the physical qubits required to factor 2048-bit RSA integers from $\sim 10^6$ to $\lesssim 10^5$. However, no demonstrations of even the most basic qLDPC operations have been made to date, and the non-local stabilizer checks in the QEC cycles impose a greater challenge to the moving of atoms [18–20]. Although the logical operations in qLDPC patches can be accelerated via lattice surgery [21–24], the recent reports of lattice surgery via the surface code on the neutral atom platform also demonstrates that logical information is lost quickly during each round of the measurement in the lattice surgery cycle [25]. The classical

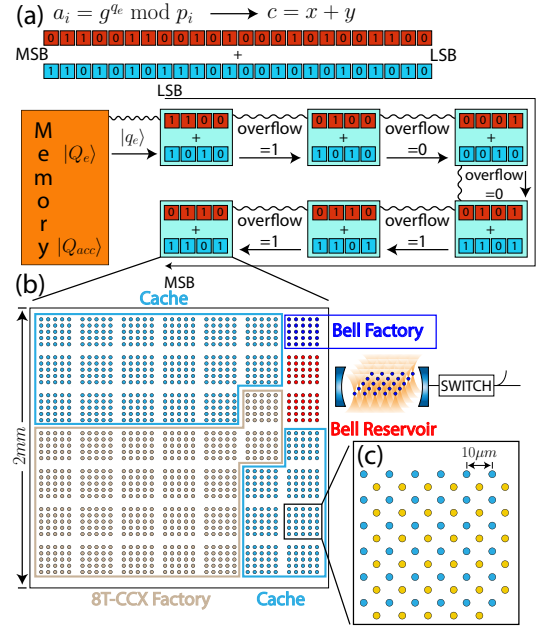


FIG. 1. Architecture of the DShor algorithm. The architecture of the modular QPU is designed around the modular exponentiations. (a) The modular exponentiation can be decomposed to modular additions and distributed to different QPUs. The addition between two 24-bit integers (red squares and blue squares) is distributed to six modules, and the additions only need local communications to ripple the overflow information to the neighboring module. (b) Each QPU in the modular processor is divided into caches, the CCX factory, and the communication zone. Temporary results of Shor's algorithm are stored in caches and non-Clifford gates are distilled from the CCX factory. Inter-module communications are created by the communication atoms (blue dots) in the cavity, which connects to the neighboring modules, and are stored in the Bell reservoir (red dots). (c) **Logical qubits are stored in the surface code patches where light blue dots represent QEC data qubits and yellow dots represent QEC ancilla qubits.** The separation between data qubits is $10\ \mu\text{m}$, and the separation between data and ancilla qubits is $5\ \mu\text{m}$.

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decoding time ($\sim 30 - 100$ ms) of qLDPC also significantly slows the circuit time [26–28]. Although these challenges are likely to introduce substantial time overheads, these high-rate codes suggest that future quantum computers are capable of tackling RSA 2048 could operate with $\lesssim 10^5$ physical qubits, and we anticipate that better decoding schemes and atom control techniques may reduce the time of logical operations in qLDPC codes to the ms level in the future.

Under the current state-of-the-art for hardware development and quantum error correction, we believe that a balance between the time and space overhead trade-off is the most promising in the near term to execute utility-scale algorithms with meaningful runtimes. Such a ‘hybrid’ architecture could, for instance, use qLDPC for memory operations that require ultra-sparse logic, and use surface codes with transversal operations combined with magic state cultivation for processing. The fast decoding (~ 1 ms per classical CPU core) and local connectivity of the surface codes allow a much faster QEC cycle [29]. As such, we believe that it is crucial to architect a balanced quantum processor to factor 2048-bit RSA integers at the requisite scale of several 100,000 physical qubits.

At this scale of physical resources, we believe that modularity of some kind will be required. We envision four possible flavors for such modularity: 1) photonic interconnects between modules in separate vacuum chambers [30–35], 2) many separate microscope objective-defined modules in the same vacuum chamber that are connected with transportable atom arrays, 3) many layers in a stack of two-dimensional modules that are integrated into a three-dimensional structure [36–38] that could involve optical lattices [39–42], and 4) many “tiled” regions that define sub-modules within a very large field of view of a single microscope objective system [43]. It is also quite likely that some combination of these four approaches will be used simultaneously, such as, e.g., many objective-defined modules in which each module could operate on two layers and use a tiled layout.

Regardless of the exact physical implementation, the key figures of merit are the number and functionality of the modules and the communication rate between the zones compared to the clock rate of the overall processor. This abstract picture invites a comparison with classical computing architectures. Specifically, CPU architectures are based on a small network of several all-powerful processor cores, while GPU architectures are based on a large network of many sub-processors of limited computational power. Naturally, the relative cost of intra- versus inter-module operations is a key parameter in these architectures. However, it is important to note that quantum communication for inter-module operations remains nascent and many orders of magnitude away from the required rate and fidelity, although the future is bright. Hence, we conclude that a CPU-type quantum processing architecture is a good target. Nevertheless, if the physical

overhead of each module could be substantially reduced by operating with a smaller code distance d , the GPU layout would become preferable. We also consider this architecture for $d = 9$ in anticipation of a future with physical error rates well below $\approx 10^{-4}$ and/or with advanced, co-designed decoders.

Here, we demonstrate an architecture for modular neutral atom hardware to perform factoring of 2048 bit RSA integers. We present an end-to-end compilation and optimization strategy that focuses on the interplay between the inter-module communication and the intra-module clock rate. Specifically, we decompose Shor’s algorithm to fundamental operations and we distribute all fundamental operations across the modules with mostly nearest-neighbor interactions. For instance, the addition between two integers is distributed across many modules and only needs local communications to ripple the overflow information to the neighboring module [see Fig. 1(a)]. We also present a new sub-routine for modular additions that obviates the need for a comparison circuit (see Appendix C). Additionally, we include a dynamic qubit reallocation protocol via atom movement, which helps balance dynamic resource loads associated with communication buffering and code cultivation (see Appendix F). Our architecture is based on one memory module with qLDPC-based logical encoding, and N_{QPU} “quantum processing unit” (QPU) modules with surface code-based logical encoding. We consider several different physical error rates and concomitant code distances for logical encoding, and we focus on module counts ranging between 1+2 and 1+12 with emphasis on the 1+6 case. Although our modular vision is largely agnostic to the exact physical implementation, for concreteness we focus on 1) photonic interconnects and 2) transportable super-arrays. In general, we find that realistic estimates for communication rates in both approaches are sufficient to cause only minimal increases in runtime compared to a monolithic architecture.

We emphasize that this study is not meant to accurately predict the required spacetime volume to run RSA 2048. There are simply too many choices for assumptions at a very dynamic time when both hardware capabilities and architectures as well as error correction strategies are improving on a monthly basis. Nevertheless, we are careful to consider nearly all space-like and all time-like overheads given our choice of physical error rate, QEC cycle time, and algorithmic architecture. In fact, we present results for two different physical error rates (10^{-3} and 10^{-4}) and two different QPU QEC cycle times (~ 0.25 and ~ 1 ms). The main space-like overhead that we do not rigorously consider is reservoir arrays to address atom loss. We estimate the overhead due to this in the outlook. In terms of time-like overhead, we believe that the thoroughness of our estimates, particularly in the exact circuit of 8T-CCX factory as well as additions and loadings, presents a more accurate picture than several past works and naturally leads to an inflated spacetime volume [17, 24, 44]. Our work presents the first end-to-end

analysis and simulation of large-scale integer factorization, focusing specifically on modular atomic hardware, and it provides a blueprint for the future design of large-scale algorithms.

II. HARDWARE ASSUMPTIONS AND ARCHITECTURES

The QPU architecture and the compilation of the distributed Shor’s algorithm are designed closely around the hardware of the neutral atom array platform. Neutral atom arrays are a leading candidate for DShor due to their relative scalability to 6,000 qubits and counting [43, 45], their access to efficient optical interconnects via optical cavities [30–34, 46], their versatile geometry [36, 47, 48], and their robust transportability for intra- and inter-module connectivity [49–51]. In this section, we will introduce the hardware assumptions and the corresponding QPU architecture used in DShor.

DShor is designed based on the ability to perform disparate tasks simultaneously. Specifically, dissipative operations such as readout and network attempting must be performed in parallel with coherent operations. For simplicity, we assume a “dual species” atom array system as illustrated in Fig. 1(c), where the atoms of the two species separately serve as data (light blue dots) and ancilla (yellow dots) qubits. Here, “dual species” is broadly defined, and could be two actual atomic species [52, 53], the ‘omg’ architecture with a single alkaline earth(-like) species [35, 54–57], or a zoned single-species system [51, 58, 59] that utilizes ‘shielding’ via local light shifts [25, 60, 61]. The separation between atoms of the same species is assumed to be $10\text{ }\mu\text{m}$, and the separation between atoms of different species is $5\text{ }\mu\text{m}$. Therefore, one logical patch with the code distance d has the dimension $10d \times 10d\text{ }\mu\text{m}^2$. We assume atoms can move at the speed of 1 m/s , and atoms are entangled by Rydberg gates. For simplicity, we assume that Rydberg gates can be applied anywhere in the workspace. We note that it remains an open question how to optimally perform stabilizer measurements in zoned architectures. Logical CNOTs are applied by moving the control logical patch close to the target logical patch followed by the transversal Rydberg gates [25, 59]. Since Rydberg gates are fast ($\approx 300\text{ ns}$) [56, 62], the gate time of the logical CNOTs is dominated by the moving time of atoms, and we approximate the gate time of logical CNOTs as $10(d+1)\text{ }\mu\text{s}$. This gate time is defined as the “clock time” in DShor and used to calibrate the gate time of all Clifford gates. See Appendix A for further details. All single-qubit Pauli gates are ignored as they can be applied without any cost by changing the Pauli frame [63, 64]. We assume a QEC cycle is applied after each logical gates although QEC cycles can be skipped if the logical error per round is lower than the target logical error [65].

As the QEC cycle of the surface code only requires local interactions, the cost of one QEC cycle is dominated by

the measurement time [66–68]. Measurement remains a major bottleneck in the neutral atom community, and we thus consider two different measurement times for full generality. The bottleneck stems from the slow laser cooling rate for tweezer-confined atoms, owing in part to the low trapping frequency ($\approx 10 - 100\text{ kHz}$). Measurement that retains the atom with high fidelity and keeps the atom cold enough to immediately be reused takes $\approx 1 - 10\text{ ms}$ [55, 60]. Measurement that either does not retain the atom or does not keep the atom cold can be performed in $\approx 20\text{ }\mu\text{s}$ [56, 57, 69, 70], but then re-cooling or obtaining a new atom from a reservoir array is required, which may take $\approx 1\text{ ms}$. Here, we consider measurement times of $\approx 250\text{ }\mu\text{s}$ (matching the logical CNOT time. More details in Appendix I) and 1 ms . Although the latter is realistic now, we also consider the former because improvements in qubit readout are expected, based on innovations such as optical cavity arrays [46, 71, 72] or confocal cavity QED microscopes [73–75].

The layout of the processor in the QCPU architecture is shown in Fig. 1(b). Each QPU can execute complicated tasks such as multi-bit additions/loadings, so **16 (+4 inputs) logical qubits are assigned to the 8T-CCX factory to distill non-Clifford gates.** As mentioned above, we consider two different inter-module connections: photonic connections and connections via transportable arrays. With photonic connections, one logical qubit patch is used to generate inter-module Bell pairs, which are saved in the Bell reservoirs with two logical qubits to buffer inter-module communication delay. The rest of the qubits are used as caches to store all intermediate results. To reduce the space used by DShor and increase the parallelism within modules, we allow qubits to be dynamically allocated between the 8T-CCX factory and the cache. Qubits are moved from the factory to the cache at intensive cache use to reduce the space usage, and qubits are moved from cache to factory on light cache use to boost non-Clifford gate production. More details of reallocation of qubits are shown in Appendix F.

With the hardware assumptions based on the neutral atom platform and the QCPU modular architecture, DShor can factor 2048-bit RSA integers with a half-million modular processor with 6 QPUs and 1 quantum memory. Since the circuit volume of Shor’s algorithm to factor 2048 bit RSA integers is $\sim 10^{13}$, a fault-tolerant quantum algorithm is required with the current physical gate error of $p_p = 10^{-3}$ or 10^{-4} . The target logical error is $p_l = 10^{-15}$, so the probability of a logical error-free shot is $\sim 99\%$. As computations only happen to a limited number of qubits at a given time (hot qubits), all idle qubits are stored in qLDPC in the memory, and hot qubits are stored in the surface code, for which we consider a few values of d , to reach the target logical error.

To reduce and balance the communications used by DShor, all intermediate results are distributed evenly to the caches of QPUs. Shor’s algorithm can be decomposed to short modular exponentiations and then decomposed further to modular additions. Since the k -

Qubit function	Qubit name	N_L	N_L (RSA 2048)	N_p (RSA 2048)	Distribution in DShor
Superposition of all exponents	$Q_{exponent}$	$n/s + n/2$	1280	100,000	in memory
Exponent in short logarithm	q_e	$ p_i $	24	30,000	$ p_i /N_{QPU}$
Result of approximate exponentiation	Q_{acc}	f	36	45,000	in memory
Result of exponentiation of single p_i	q_r	$ p_i + 1$	25	31,250	$(p_i + 1)/N_{QPU}$
Intermediate result of multiplication	q_h	$ p_i + 1$	25	31,250	$(p_i + 1)/N_{QPU}$
Temporary memory of table values	q_l	$ p_i + 1$	25	31,250	$(p_i + 1)/N_{QPU}$

Table I. **Qubit allocation in DShor.** $Q_{exponent}$ and Q_{acc} are stored in the memory, and all intermediate results used by DShor is distributed evenly to all QPUs. N_L is the number of logical qubits to store the result, and N_p is the number of physical qubits required at $d = 25$.

th bit in the result of additions $r = x + y$ depends only on the current adding bits and the overflow bit: $r_k = x_k \oplus y_k \oplus c_{k-1}$, $c_k = \text{MAJ}(x_k, y_k, c_{k-1})$, where $\text{MAJ}(x_k, y_k, c_{k-1})$ is the majority gate, which returns the majority bit among (x_k, y_k, c_{k-1}) , additions only require local (nearest-neighbor) communications to propagate the overflow information c_{k-1} [76]. In Fig. 1(a), the exponent $|q_e\rangle$ of the modular exponentiation $|g^{q_e}\rangle$ is read from the quantum memory, and the modular exponentiation is decomposed to additions. All bits involved in the additions are evenly distributed to QPUs, and the overflow information is rippled through all QPUs by a cascade of local communications. More discussion of the distributed operations in DShor can be found in IIIB.

III. THEORY AND METHODS

A. Shor's algorithm with residue arithmetic

In this study, we focus on the Shor's algorithm using the residue arithmetic to reduce the number of qubits used [2]. Shor's algorithm roots at the modular exponentiation:

$$\sum_e |e\rangle \rightarrow \sum_e |e\rangle |g^e \bmod N\rangle \quad (1)$$

Therefore, Shor's algorithm needs to store all exponents $|e\rangle$ and all results $|g^e \bmod N\rangle$. The naive Shor's algorithm requires at least $2n$ qubits to factor n -bit integers ($|N| = n$). The size of exponents can be reduced to $n/2 + n/s$ qubits in RSA integers, and the number of hot qubits required by modular exponentiations can be reduced to $O(\log(n))$ by the residue arithmetic [2, 4].

As most computations in Shor's algorithm are modular exponentiations, we focus on the simplification and distribution of modular exponentiations in this paper. The modular exponentiation of $g^e \bmod N$ can be decomposed to multiple short modular exponentiations from a prime system $\{p_i | \gcd(p_0 \dots p_n) = 1\}$ and a residue system $\{a_i = g^k \bmod p_i\}$:

$$g^e = \sum_i a_i P_i r_i \quad (2)$$

where $P_i = \prod_{j \neq i} p_j$, $r_i = P_i^{-1} \bmod p_i$, and $\prod_i p_i \gg N$. Both P_i and r_i can be found classically, and only $\{a_i\}$

are calculated on the quantum computers. Therefore, the number of qubits required for results is $|p_i| = \log n$, which significantly reduces the space required by the Shor's algorithm. More details and further simplifications of Shor's algorithm using the residue arithmetic can be found in Appendix D.

In DShor, qubits storing exponents $|Q_{exponent}\rangle$ and the result $|Q_{acc}\rangle = |\sum a_i P_i r_i\rangle = |g^e \bmod N\rangle$ are stored in the quantum memory, and all qubits required for the modular exponentiations $|a_i\rangle = |g^e \bmod p_i\rangle$ are evenly distributed to all QPUs as shown in Fig. 2(a). Qubits in the quantum memory are stored in [510, 16, 24] generalized bicycle (GB) code with w_1 surface code patches to extract the information from qLDPC by general lattice surgery [16, 24, 66, 77]. In DShor, we assume all qubits are stored in a single-module memory, but the memory can be split into multiple modules as needed based on the hardware implementation. Splitting the memory into more modules has a negligible effect on the DShor due to the infrequent usage of qubits in the memory. To factor 2048 bit RSA integers, 80 GB code patches and 12 surface code patches (to read information from the memory), or 96,600 physical qubits, are required. We round it up to 10^5 to buffer additional qubits used for lattice surgery. The exact space usage of DShor to factor general RSA integers and 2048 bit RSA integers is shown in Table. I

The Shor's algorithm with the residue arithmetic can be constructed with the following five subroutines: loading exponents, qubit compression, modular exponentiation, accumulating results to the memory, and memory & phase cleaning as shown in Fig. 2(b) [2]. In DShor, we further decompose the five subroutines to three fundamental operations: loading, adding, and cleaning. Loading transfers classical information $f(e)$ to quantum registers depending on the quantum address $|e\rangle$:

$$|e\rangle |0\rangle \rightarrow |e\rangle |f(e)\rangle \quad (3)$$

Adding applies a direct addition on two quantum registers:

$$|a\rangle |b\rangle \rightarrow |a + b\rangle |b\rangle \quad (4)$$

And cleaning resets all temporary quantum memories for the future reuse:

$$|a + b\rangle |b\rangle \rightarrow |a + b\rangle |0\rangle \quad (5)$$

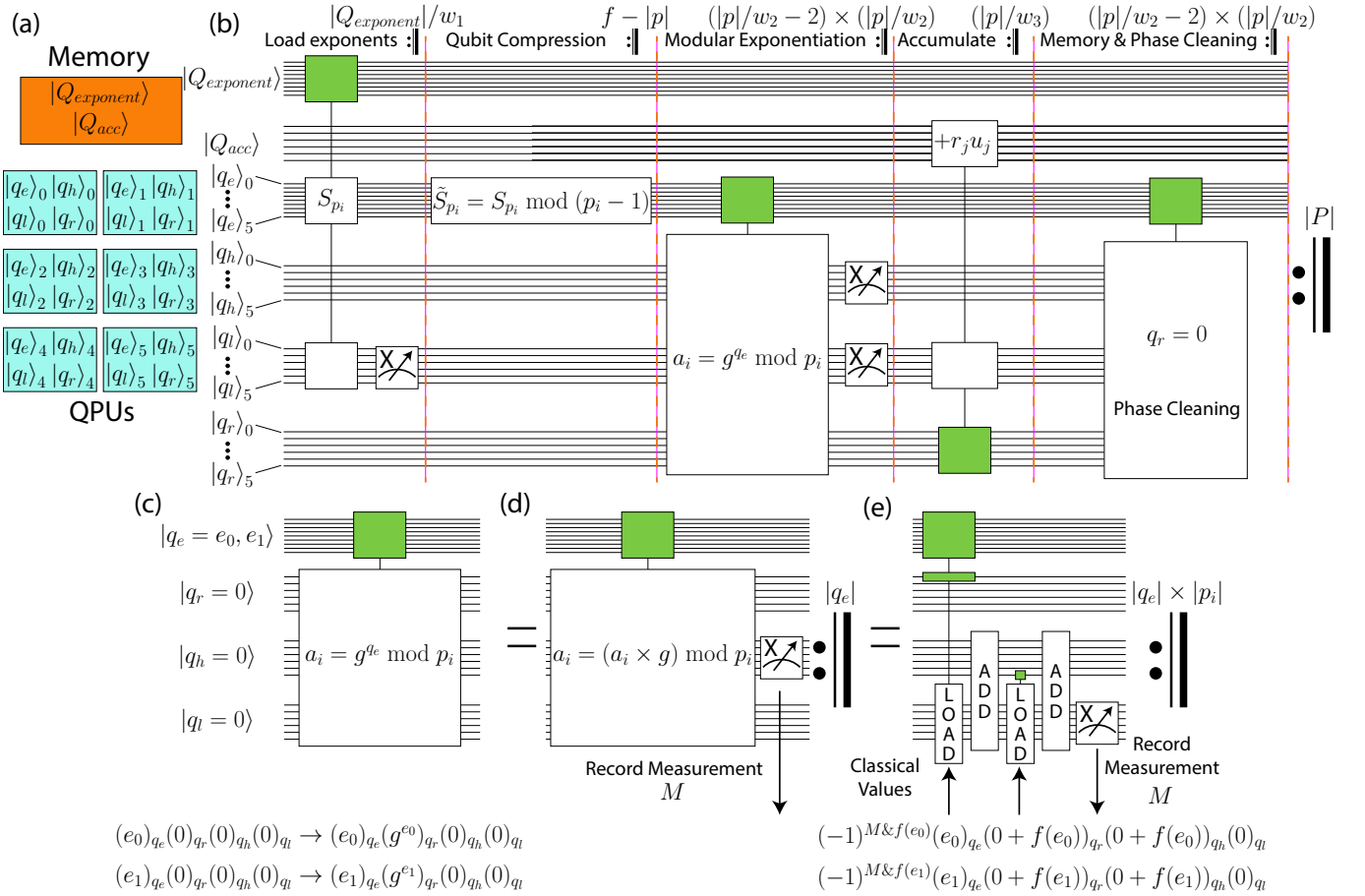


FIG. 2. **Algorithmic structure of DShor.** (a) Results of Shor's algorithm are stored in the memory (the orange square), and all intermediate results are distributed evenly to all QPUs (blue squares). (b) Shor's algorithm is decomposed to five steps: 1. loading short logarithms from the memory to the QPUs, 2. compressing the short logarithms, 3. modular exponentiations, 4. accumulating results to the memory, and 5. cleaning all intermediate results and phases. The whole procedure is iterated over all primes in the prime system. (c) The circuit of DShor is simulated and verified by the Shor's simulator. When the modular exponentiation g^{q_e} is implemented, it will be decomposed to modular additions by the compiler. The simulator initializes the limited number of tracked Hilbert trajectories (such as the trajectory with $|q_e = e_0\rangle$). The modular exponentiation is decomposed to (d) $|q_e|$ modular multiplications and then to (e) $|q_e| \times |p_i|$ modular additions. Modular additions are further decomposed to fundamental operations (loading+adding+cleaning). Each time a fundamental operation is implemented, the front-end circuit simulator will evolve the circuit, and the back-end simulator will update the Hilbert trajectories. At the end of the modular exponentiation, the simulator will check if all trajectories are $|q_e\rangle \otimes |g^{q_e}\rangle$. The final circuit after the verification is used for the resource estimation.

A naive decomposition of modular exponentiation to fundamental operations is in Fig. 2(c,d,e), where one modular exponentiation g^{q_e} is decomposed to $|q_e|$ modular multiplications and further to $|q_e| \times |p_i|$ modular additions with two additions and two loadings. The detailed decomposition of Shor's algorithm to fundamental operations can be found in Appendix B, C, E, and G.

B. Distributed fundamental operations

As noted in the introduction, Shor's algorithm needs to be distributed over modules at the current stage of quantum computers. Shor's algorithm can be decomposed to modular additions and further to fundamental operations

as shown in III A, so the distribution of Shor's algorithm can be simplified to the distribution of fundamental operations.

All fundamental operations in DShor can be efficiently distributed using qubit and gate teleportation, which are transversal operations at the logical level and thus each consume d^2 physical Bell pairs. In Fig. 3, we demonstrate the distribution of loading and adding, and the distribution of cleaning can be found in Appendix E. In Fig. 3(a), a loading gate is distributed over 2 QPUs, and the naive compilation of loading requires $|q_l|/2$ communications. We decompose one loading gate (one cascade of CNOTs) with two pre-loading gates on two qubits of a Greenberger-Horne-Zeilinger (GHZ) state. One qubit in a GHZ state is used to record the information of

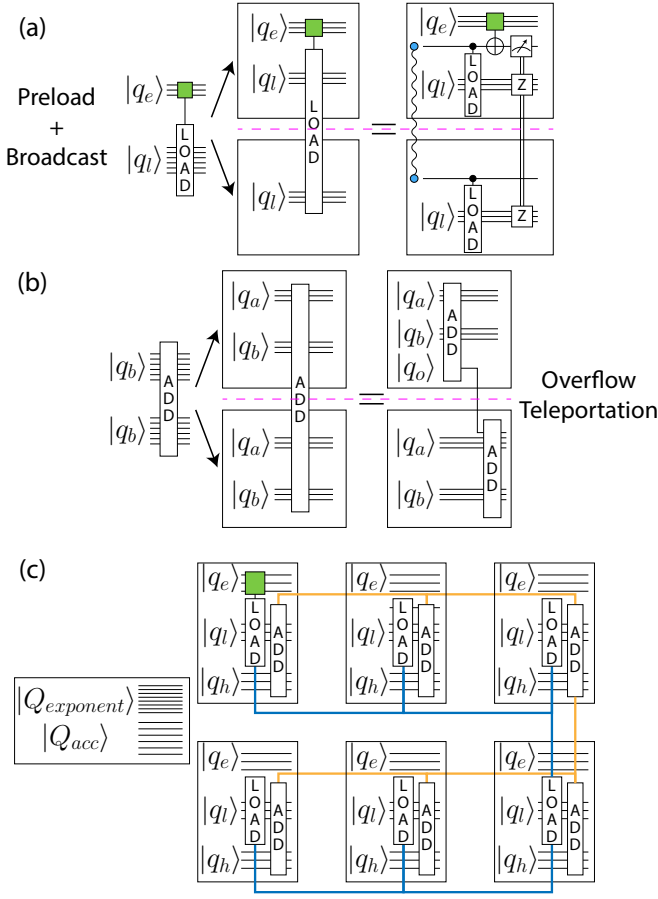


FIG. 3. **Distributed fundamental operations of DShor.** (a) Loadings transfer classical information to the quantum registers depending on the quantum address (green square) $|q_e\rangle$. Loading is distributed by N_{QPU} intra-module pre-loadings, and the quantum address is broadcast to all modules through one inter-module GHZ state. (b) Adding sums two quantum registers, and it is distributed by teleporting the overflow information to the neighbor module. Un-Adding is skipped in (b) for the cleaner illustration. (c) Modular exponentiation can be decomposed to one loading and two additions, which can be distributed with only local (nearest-neighbor) communications. Each loading requires one GHZ state across modules as labeled by the blue lines, and the addition requires the ripple teleportation of the overflow information, which is labeled as yellow lines.

the addresses read from the quantum registers and then broadcast the information to all QPUs through the GHZ state in which it resides via gate teleportation [7]. The distributed loading reduces the communication from $|q_l|$ non-local communications to 1 GHZ state, or 1 local communications between the neighboring QPUs.

Addition ladders have exhibited good distributivity as mentioned in Section II, where 3 local communications are required for both the addition and the un-addition (cleaning of all temporary memories) [76]. We replace 3 local communications with 1 local communications by the qubit teleportation as shown in Fig. 3(b). The exact

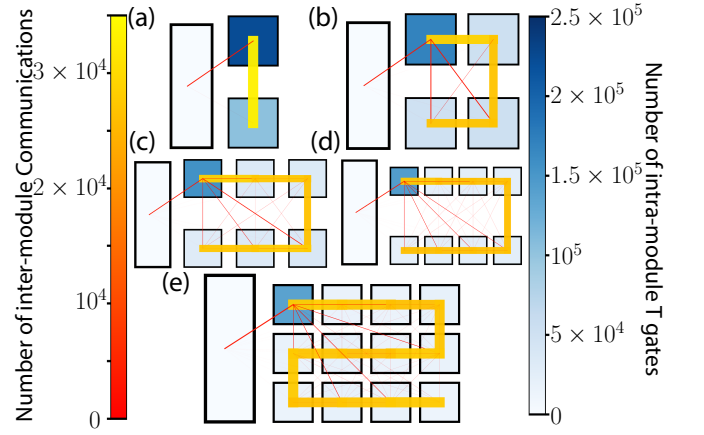


FIG. 4. **Inter-module communications and the T gate count in DShor.** We simulate the DShor to factor 2048-bit RSA integers with 2, 4, 6, 8, 12 QPUs in (a)-(e), respectively. The rectangle on the left is the quantum memory, and the squares on the right are QPUs. The white-to-blue color scale (right) of the rectangles and squares represents the total number of T gates used in each Shor's shot, and the red-to-yellow color scale (left) and thickness of lines represents the communications between modules. Except the 2-QPU DShor, the communications between modules are roughly unchanged with the number of QPUs in DShor, but the number of intra-module T gates per module decreases as DShor is distributed to more QPUs. The QPU with significantly more T gates is the router QPU, which reads and loads the quantum registers from the memory. Most connections in DShor are local communications as the fundamental operations only require local communications.

circuit of distributed loading and addition can be found in Appendix E.

As the fundamental operations can be distributed with local communications, modular additions can also be distributed with only local communications as shown in Fig. 3(c), where the blue lines label 1 GHZ state consumed by the loading and the orange lines label the trajectory of qubit teleportations of one addition. In Fig. 4, we show that the vast majority of communications needed for DShor when built from fundamental operations are local (nearest-neighbor). The widths and colors of lines connecting all QPUs indicate the number of communications between QPUs. If address qubits of loadings are not in the neighbor modules, a non-local qubit teleportation is used to teleport all address qubits into the same module, which leads to few non-local communications in DShor. Here, we assume all-to-all connections among QPUs. However, to factor RSA 2048 integers with 6 QPUs, only 5% of connections are non-local, which has a negligible effect on DShor if all non-local connections are distilled by GHZ states created by local connections [78]. Most of the non-local connections are from the address teleportations during the modular multiplications. We elaborate on the amount of inter-module communications and intra-module T gates in Section IV.

C. Simulation method

To verify our decomposition of Shor’s algorithm to fundamental operations, we invent a Shor’s simulator that can simultaneously evolve the front-end circuit and track the back-end Hilbert trajectories. To simulate Shor’s algorithm in large systems, we only track a limited number of trajectories in the Hilbert space. In the naive decomposition of modular exponentiation shown in Fig. 2(c,d,e), two Hilbert trajectories with different exponents $|q_e\rangle$ are tracked, and the modular exponentiation $|q_e \bmod p_i\rangle$ is calculated on $|q_r\rangle$. All classical information is loaded on $|q_l\rangle$ and intermediate results are saved in $|q_h\rangle$. All registers except those storing $|q_e\rangle$ are initialized to $|0\rangle$. More details of the resource estimation methods used in the Shor’s simulator are in Appendix. H

In our resource estimation of Shor’s algorithm of RSA 2048, 32 random Hilbert trajectories are tracked. Modular exponentiations in the DShor are decomposed to fundamental operations, which evolve the circuit and the backend trajectories. For example, the modular additions will be decomposed to two additions, two loadings, and one cleaning (Fig. 2(e)). Additions and loadings will evolve the Hilbert trajectory to $|e\rangle_{q_e} |0 + f(e)\rangle_{q_r} |0 + f(e)\rangle_{q_h} |0 + f(e)\rangle_{q_l}$. The classical values of $|q_l\rangle$ are removed by transversal X measurements. Each trajectory will get a phase error depending on the measurement result and the loaded classical values, which will be cleaned later. Therefore, after one modular addition, the Hilbert trajectories will evolve to $(-1)^{M \& f(e)} |e\rangle_{q_e} |0 + f(e)\rangle_{q_r} |0 + f(e)\rangle_{q_h} |0\rangle_{q_l}$, and the circuit of the modular addition is also recorded. Accordingly, the circuit of modular exponentiations can be verified by checking if all evolved trajectories reach $|e\rangle |g^e \bmod p_i\rangle$ without phase errors. A detailed implementation of Shor’s simulator on the modular exponentiation is shown in Appendix. G

IV. DSHOR ON THE ARRAYS WITH PHOTONIC INTERCONNECTS

1. Choice of parameters

We simulate DShor on the canonical RSA 2048 challenge and specially design the parameters suitable to DShor as shown in Table I. In DShor, each QPU requires at least $4|p_i|/N_{\text{QPU}}$ qubits to store all intermediate results. As the optimal size of primes is $O(\log(N))$, we choose $|p_i| = 24$ for the QCPU modular architecture. We heuristically set the window size of loading short logarithm as $w_1 = 6$ and the window sizes of modular exponentiations and multiplications as $w_e = w_m = 3$ to minimize the time of DShor. More data of DShor at different window sizes can be found in Appendix I.

2. QPU connectivity, strong scaling analysis

We apply DShor on 2, 4, 6, 8, 12 QPUs to factor 2048 bit RSA integers using the parameters mentioned above and estimate the space and time usage from the circuit evolved by the Shor’s simulator as shown in Fig. 5. We assume that the physical error is 10^{-3} and benchmark our gate time to $250 \mu\text{s}$ as mentioned in Section II. Although QEC cycles are not necessary after each logical operations [65], we assume all logical operations are followed by one QEC cycle to provide the worst-case resource estimate. The QEC cycle time is estimated as the measurement time, as discussed in Section II. Although increasing the number of qubits per module can accelerate the algorithm, we use the minimal spacial resources in the QPU (only one CCX factory) for our resource estimation. The delay τ from inter-module communications is benchmarked by the clock time: $\tau \equiv \frac{t_{\text{inter}}}{t_{\text{intra}}}$. The circuit time is benchmarked by the single-module Shor’s algorithm with 180 hot qubits, which has circuit depth 2.25×10^{10} and circuit time of 164.5 days per shot.

We estimate the inter-/intra-module resources used by DShor with 2, 4, 6, 8, 12 QPUs to factor 2048 bit RSA integers in Fig. 4. The rectangles on the left are the quantum memories, and the squares on the right are QPUs. Memory is only accessed during two steps of DShor: *load exponents* and *accumulate results*. During *load exponents*, $w_1 = 6$ qubits from the exponents $|Q_e\rangle$ are read to the buffer surface code patches by the lattice surgery, and the buffer patches are teleported to the “router” QPU. Short logarithms $|q_e\rangle$ are then computed based on these six buffer qubits in the router QPU, and the short logarithms $|q_e\rangle$ are used for modular exponentiations. When the modular exponentiation is finished, the result of approximate exponentiation $|Q_{\text{acc}}\rangle$ is teleported to all QPUs to record the current result of modular exponentiation $|q_r\rangle$. Therefore, all calculations happen in the QPUs, which leads to 0 T gates in the memory. More details about memory access in DShor can be found in Appendix H.

Except the router QPU (the upper-left QPU with more T gates), each QPU uses a similar number of T gates, and the number of T gates per QPU decreases as the number of QPUs used in DShor increases. The “router” QPU has more T gates as all information from the memory is processed by the “router” QPU. The amount of communications between modules remains roughly unchanged with the number of QPUs in DShor, and most of the communications are local as discussed in Section IIIB.

We also estimate the strong scaling of RSA 2048 DShor as shown in Fig. 5, and the circuit time is benchmarked by the circuit time of the single-core Shor’s algorithm with 180 qubits and 1 ms measurement time: $t_0 = 164.5$ days. Figure 5(a) shows that the circuit time of DShor increases linearly with the communication delay τ , and the circuit time of DShor with 6 QPUs is approximately the same as the single-core Shor’s algorithm at $\tau = 10$, which we refer as “free modularization”. The delay of DShor is more significant as the cost of communications increases since the

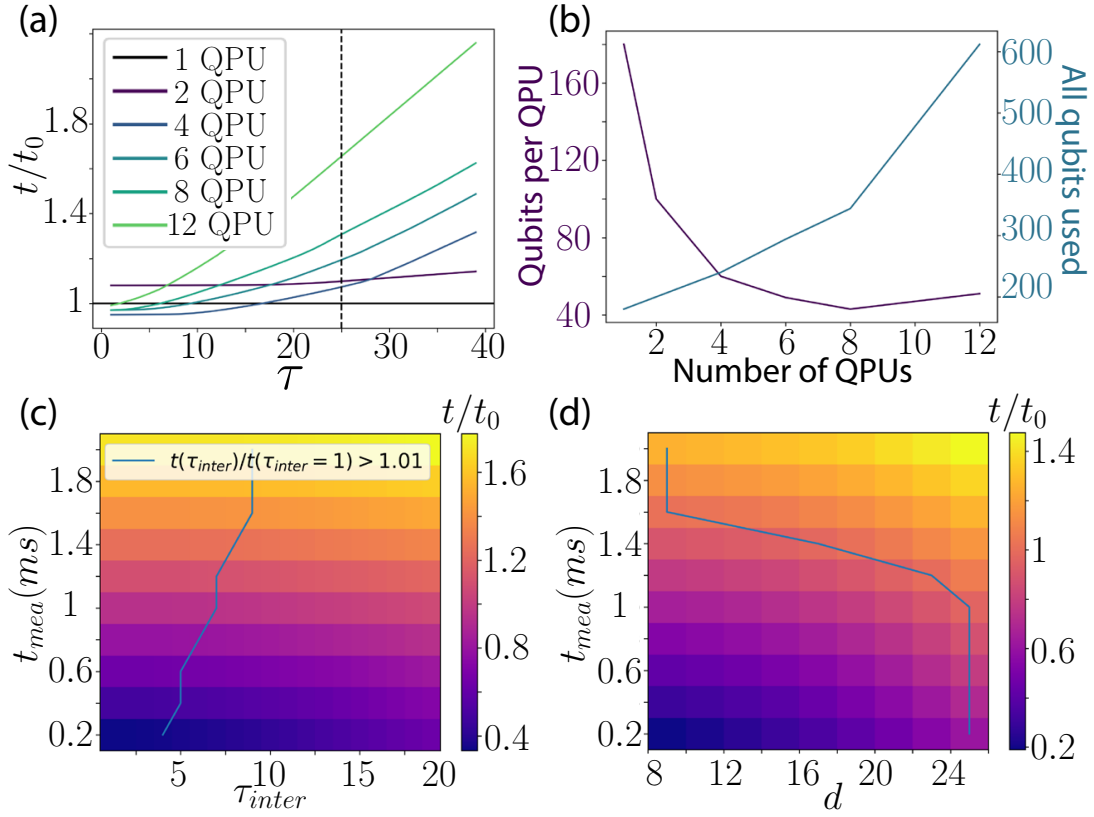


FIG. 5. **Results of DShor.** We estimate the space and time usage of the DShor with 2, 4, 6, 8, 12 QPUs to factor RSA 2048-bit integers. The circuit time is benchmarked by the circuit time of single-core Shor’s algorithm with 180 qubits: $t_0 = 164.5$ days. (a) The circuit time of DShor with 2, 4, 6, 8, 12 QPUs at different costs of inter-module communications, where the communication cost is benchmarked by the cost of logical intra-module CNOTs (without QEC) time: $\tau = \frac{t_{inter}}{t_{intra}}$ and $t_{intra} = 250\mu s$. $\tau = 25$ corresponds to 10^5 physical inter-module Bell pairs generated per second as labeled by the dashed black line. DShor gains small advantage at low communication cost, and the delay from the inter-module communications is more significant as more QPUs are involved in the DShor. The circuit time of 6-QPU DShor with communication rate 10^5 Bell pairs/sec is 16% longer than the single-module Shor. (b) The strong scaling of DShor at different number of QPUs (excluding memory). The purple line represents the qubits per QPU, and the blue line represents the total number of qubits used. The qubits used per QPU decreases with a diminishing slope. The qubits per QPU reaches the minimum at 8 QPUs and increases at 12 QPUs as more qubits are required to accommodate the frequent communications and teleportations in the DShor. The total number of qubits used increases roughly linear with the number of QPUs with a sudden increase at 12 QPUs. (c) The circuit time of 6-QPU DShor at different communication cost and measurement time. The measurement time is also benchmarked by the time of logical intra-module CNOTs (without QEC): $\tau_{mea} = \frac{t_{mea}}{t_{intra}}$. The distribution of Shor’s algorithm is not delayed by the inter-module communications to the left of the blue line (“free modularization”), where $t(\tau_{inter})/t(\tau_{inter}=1) < 1.01$. The threshold of “free modularization” also increases with a higher measurement time since more operations can happen in parallel behind the measurement.

longer inter-module communications delay more subroutines. The space used by DShor is illustrated in Fig. 5(b), where the purple curve represents the number of qubits within one QPU, and the blue curve represents the total number of qubits in the modular processor. The number of qubits within one QPU decreases with a diminishing slope. The number of qubits per QPU increases when DShor is distributed to 12 QPUs as each QPU requires more qubits to buffer the frequent qubit teleportations in the DShor. We focus on the analysis of 6 QPU DShor to factor 2048-bit RSA integers with $p_p = 10^{-3}$, so each QPU has 7×7 logical qubits and 61,250 physical qubits in a 2×2 mm² atom array workspace, which we believe

is a realistic field of view based on the current state-of-the-art for microscope objectives [43, 45].

We also estimate DShor for different physical error rates and associated gate times and different RSA challenges with constant communication rate 10^5 physical Bell pairs per second, as shown in Table. II. This communication rate is based on recent predictions for multiplexed and parallelized cavity-based networking protocols [34, 35, 46]. Here, we only consider the time required for one shot of Shor’s algorithm. The expected number of classical shots required to factor RSA 2048 integers is 9.2 at $s = 8$, and all shots can be collected by 10 identical modular quantum computers working in parallel or

	Code distance	N_L	N_p	Total qubits used (excluding memory)	Clock time $10d \mu s$	t_{mea} (ms)	Comm. rate (ebits/s)	Time (one shot)	t_0 (days)
RSA 1024 ($p_p = 10^{-3}$)	23	40	38,088	296,240	230	1	10^5	27.4 days	17.1
RSA 1024 ($p_p = 10^{-4}$)	14	40	14,112	109,760	140	1	10^5	21.6 days	15.9
RSA 2048 ($p_p = 10^{-3}$)	25	49	61,250	367,500	250	1	10^5	190.4 days	164.5
RSA 2048 ($p_p = 10^{-3}$)	25	49	61,250	367,500	250	0.25	10^5	130.3 days	65.2
RSA 2048 ($p_p = 10^{-4}$)	15	49	22,050	132,300	150	1	10^5	148.3 days	151.6
RSA 2048 ($p_p = 10^{-3}$)	15	49	22,050	132,300	150	0.25	10^5	63.8 days	52.3
RSA 4096 ($p_p = 10^{-3}$)	27	49	71,442	428,652	270	1	10^5	1085.3 days	1062.1
RSA 4096 ($p_p = 10^{-4}$)	16	49	25,088	150,528	160	1	10^5	908.2 days	972.7

Table II. Resource usage in DShor. We estimate the space and time usage of DShor with 6 QPUs to factor (1024, 2048, 4096 bit RSA integers) at physical errors $p_p = 10^{-3}$ and $p_p = 10^{-4}$. We record the number of logical qubits (N_L) and physical qubits (N_p) per module, and we assume the communication rate between modules is $10^5/s$ physical Bell pairs. t_0 represents the circuit time of the DShor with 180 logical qubits with the measurement time t_{mea} . In DShor, the time of one logical operations (CNOT, H, S, etc.) at least needs $t_{mea} + 10d\mu s$. Therefore, the circuit time of DShor does not change significantly with the code distance given the long measurement time, which becomes a significant parameter influencing the circuit time. The circuit time of single-core Shor’s algorithm (t_0) suggests this trend, where $t_0(t_{mea} = 250 \mu s)/t_0(t_{mea} = 1 ms) = 65.2/164.5 = 0.396$. The ratio of logical operation times at $t_{mea} = 250 \mu s$ and $t_{mea} = 1 ms$ is $500 \mu s/1.25 ms = 0.4$, which is almost the same as the circuit time ratio. For the DShor with 6 QPUs, the circuit time is less sensitive to the measurement time as the latency from the inter-module communications becomes a significant bottleneck at short measurement time as shown in Appendix I.

by using 6×10 QPUs connected to the shared memory [2, 4, 79–81]. s is the Ekerå’s parameter to control the space and time tradeoff. Shor’s algorithm requires $N/2 + N/s$ qubits in the memory and $\sim s + 1$ classical shots. The compilation of DShor in the QGPU architecture (~ 100 modules) can be found in Section VI.

The circuit time of Shor’s algorithm strongly depends on the measurement time, as shown in Fig. 5(d), since the time of the QEC cycle depends on the measurement time. Fig. 5(d) shows the circuit time of 6-QPU DShor to factor 2048-bit RSA integers at different measurement time τ_{mea} and communication delay τ_{inter} . The QEC cycle is longer as the measurement increases, and further increases the running time of DShor. However, the longer measurement time also gives more time for parallelism between intra-module operations and inter-module communications, which increases the threshold of “free” modularization. The blue curve captures the threshold of “free” modularization where $t(\tau_{mea})/t(\tau_{mea} = 1) \leq 1.01$. The measurement time can also significantly change the compilation of DShor. We assume measurement is much more expensive than physical gates, so logical CNOTs are implemented by transversal CNOTs instead of the lattice surgery. Therefore, the cascade of CNOTs can only be implemented sequentially, which significantly increases the circuit time. This delay can be resolved by a GHZ-empowered CNOT fanout at the price of more qubits per QPU or lattice surgery on platforms with fast measurement (e.g. superconducting circuits) [2, 7, 82]. We leave

this analysis to future work.

The resource and communications used by DShor also strongly depend on the physical error. As the physical error decreases from 10^{-3} to 10^{-4} , the code distance can decrease by ~ 10 , which can reduce the qubit usage by $\sim 60\%$ and reduce the time of DShor by $\geq 12\%$ [83]. Table II illustrates this trend, with resource estimates for both $p_p = 10^{-3}$ and 10^{-4} at each RSA challenge size. The exact code distance required at the certain physical error can fluctuate significantly depending on the physical fidelity of different gates and the decoder [29, 83–86]. However, if the target error of DShor is fixed to 10^{-15} , different decoders and physical errors only affect the target code distance, so we use the code distance as a measure of physical error and decoders. We simulate DShor with 6 QPUs with $10^5 s^{-1}$ inter-module physical bell pairs at different measurement time t_{mea} and code distance d . One shot in DShor can reach as low as 30 days per shot if $t_{mea} = 0.2 ms$ and $d = 9$. The blue line captures $t/t_0 \leq 1$.

V. DSHOR WITH DYNAMIC SUPER-ARRAYS

Besides of the compilation of DShor on the static arrays with photonic inter-module connection, we also provide the compilation of DShor on super-arrays connected by dynamic arrays as illustrated in Fig. 6(a).

We compile the 6-QPU DShor to factor 2048 bit RSA integers on seven static arrays (6 QPUs and 1 mem-

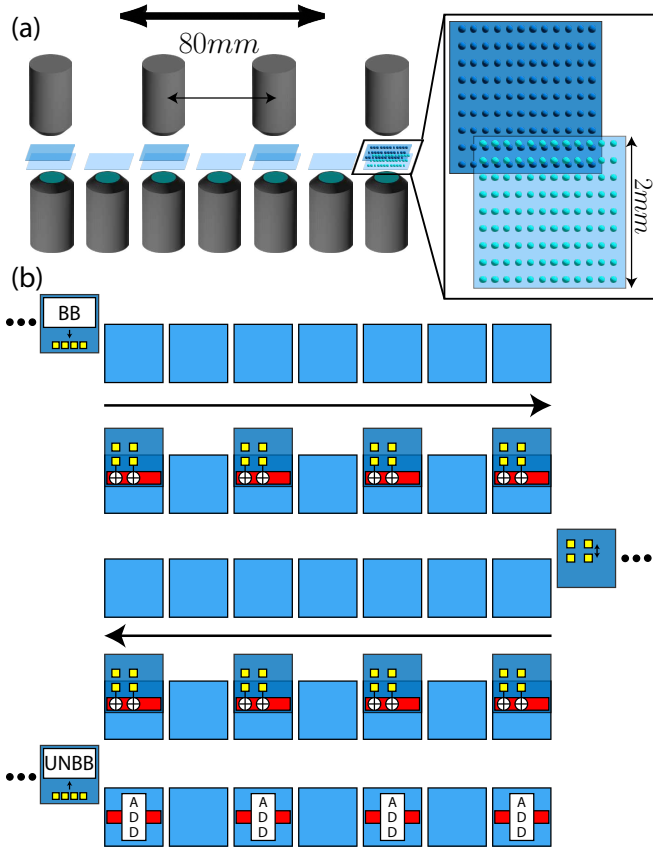


FIG. 6. **DShor on the dynamic array.** (a) The modular atomic processors connected by the dynamic arrays. Seven static arrays (six QPUs and one memory) are connected by four dynamic arrays. Each array contains a $2 \times 2 \text{ mm}^2$ atom array as illustrated in Fig. 1. The separation between the static objectives is 40 mm, and the separation between dynamic arrays is 80 mm. All dynamic arrays can move collectively and create inter-module connections when the dynamic array overlap with the static array. They all share a common focal plane. (b) Compilation of DShor on the dynamic arrays with multi-address loadings. A quantum address is loaded on the dynamic array and processed by the Bucket-Brigade circuit. Classical information is loaded to static QPUs as dynamic arrays sweep through all static QPUs. The address qubits are cleaned by Un-Bucket-Brigade circuit while the quantum addition happens in parallel.

ory) connected by four dynamic arrays. This hardware approach is nascent but provides a method to scale to several 100,000 physical qubits within a single vacuum chamber without the need for photonic interconnects. Anticipating a future in which RSA 2048 can be performed with $\sim 10^4 - 10^5$ qubits via high-rate QEC codes, we may wish to deliberately eschew the photonic interconnects between modules contained in separate vacuum chambers and adopt a single-chamber architecture. To reach the several 100,000 physical qubit scale required for our CSS code-based processor architecture, we envision defining many modules via an array of microscope objectives spaced by $\approx 40 \text{ mm}$.

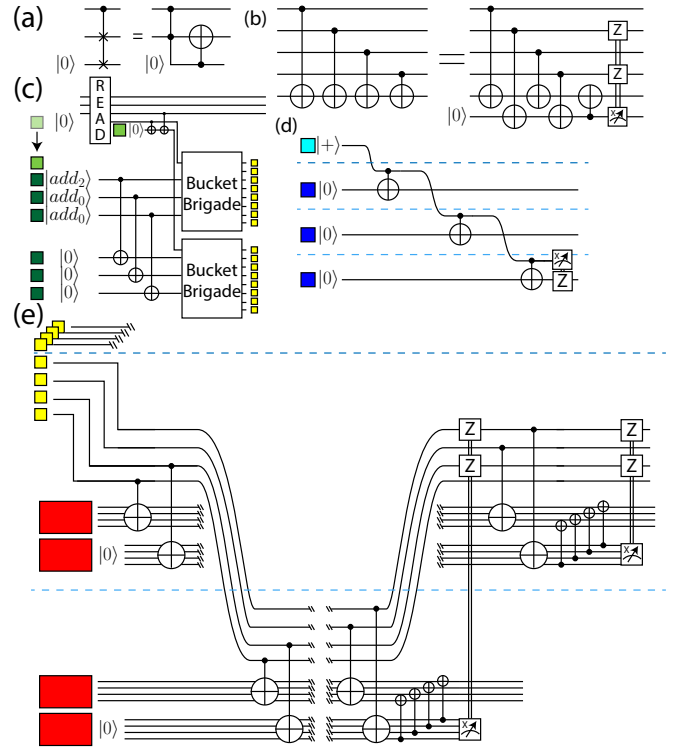


FIG. 7. **Circuit of DShor on the dynamic arrays.** (a) The controlled swap gate between one data qubit and one $|0\rangle$ in the Bucket-Brigade circuit can be simplified. (b) One cascade of CNOTs can be split to two shorter cascades of CNOTs with one ancilla qubit. (c) Hybrid quantum loadings on the dynamic array. All quantum addresses are read by unary loadings except the last three quantum addresses (dark green squares). The three quantum addresses are expanded to three Bell pairs and further expanded to 16 address qubits (yellow squares) by the Bucket-Brigade circuit. (d) A cascade of CNOTs are applied from the dynamic array to the static array to generate one GHZ state across all static arrays. (e) Quantum information is loaded from the address qubits (yellow squares) to the data registers (red squares). Each data register is accompanied by one ancilla qubit to double the loading bandwidth using the circuit in (b). Classical information is loaded from the address qubits to the data registers during one sweep of the dynamic arrays.

Communication between these modules is performed by atom arrays that can be transported between them. Dynamic objectives from the opposite side of the vacuum chamber as the static objectives are able to move together laterally via an air bearing linear motion stage on which all four of them are placed. The focal plane in which the atom arrays reside is shared by all objectives. The working principle of the optical system, though not described in detail here, is designed to preserve the full functionality of each array, both static and dynamic. Such linear motion stages are widely used in high-tech manufacturing including in extreme ultraviolet lithography, where wafer and reticle stages move in vacuum with nm-scale precision in two-dimensions with accelerations of $\sim 15g$.

For the application presented here, suitable stages with max acceleration of $2g$ and max velocity of 1 m/s are readily available, and stages with $5g$ and 5 m/s are also realistic. Here, we assume that dynamic arrays can move with maximum jerk $j = 600\text{ m/s}^3$, maximum acceleration 20 m/s^2 ($\approx 2g$) and maximum speed 2 m/s . The moving profile of the dynamic arrays is illustrated in Fig. 7. We assume both static array and dynamic arrays have dimension $2 \times 2\text{ mm}^2$ with 7×7 logical qubits, the same as in Section IV.

We assume a periodic motion profile based on zooming back and forth between the two ranges of travel such that, at one end, the fourth dynamic objective overlaps with the first static objective, and at the other end of travel, the first dynamic objective overlaps with the seventh static objective. The range of movement of the dynamic arrays can cover all static arrays as illustrated in Fig. 6(b) and can only move collectively. We assume that ‘drive-by’ Rydberg entangling gates can be performed between the static atoms in the static modules and the dynamic atoms in the dynamic modules, such that the dynamic modules do not need to start and stop at each static module which would enormously inflate the communication time. As noted above, Rydberg-mediated gates require only $\approx 300\text{ ns}$ [56, 62]. Assuming the two atoms participating in the gate are separated by $y = 5\text{ }\mu\text{m}$ and that they have a relative velocity of $v_x = 1\text{ m/s}$ perpendicular to their axis of separation, the effective change to their separation during the 300-ns gate (assuming it is centered on $x = 0$) is $\delta r \approx 2\text{ nm}$, which is completely negligible. The Doppler shifts associated with the relative motion can likewise be negligible if the Rydberg beam is perpendicular to the direction of motion. Recently, such a drive-by gate was demonstrated with state-of-the-art fidelity at a very low relative velocity of 0.05 m/s , limited by the Doppler sensitivity of the setup [87]. We also present the machine code of *loading* using the drive-by gates in Appendix K.

The dynamic array architecture can provide a very large per-pass bandwidth between modules because of the highly parallelizable transversal drive-by gates between the dynamic array and the static array. If the dynamic array has a complete overlap with the static array, all qubits on the dynamic arrays can be used to generate inter-module Bell pairs. We assume all arrays contain $7 \times 7\text{ }d = 25$ surface code patches (61,250 physical qubits as shown in Table. II), and 6 static arrays are connected by one dynamic array. One transverse move can generate 61,250 physical 6-qubit GHZ states among all static arrays, which requires 306,250 physical Bell pairs between the nearest-neighbor modules and takes 0.37 s [see Fig. 8(a)], which corresponds to a bandwidth of 8.3×10^5 physical Bell pairs per second. This exceeds all but the most optimistic estimates for photonic interconnects.

However, the bandwidth of the inter-module connections heavily depends on the size of the Bell-pair reservoir. In the architecture illustrated in Fig. 1(b) with 3 logical qubits in the Bell pair reservoir, one transverse

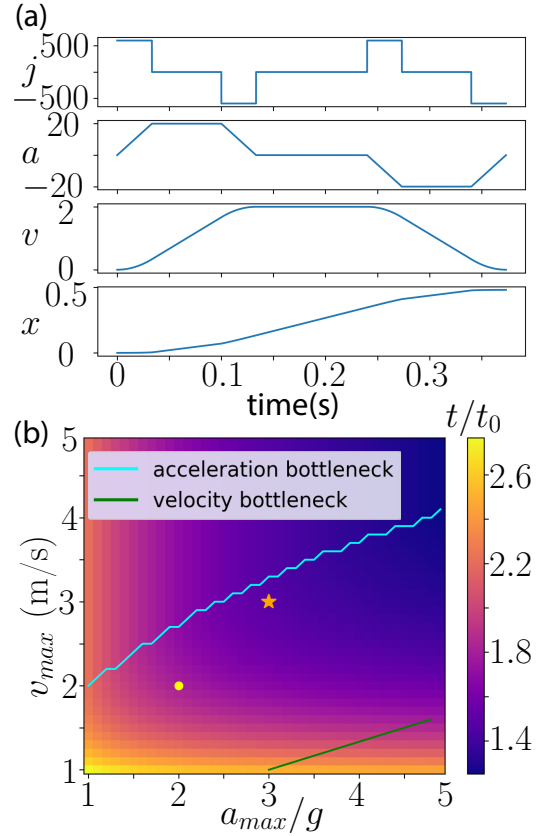


FIG. 8. **Dependence on the motion profile of the dynamic arrays.** (a) The moving profile of at $j_{\max} = 600\text{ m/s}^3$, $a_{\max} = 20\text{ m/s}^2$, $v_{\max} = 2\text{ m/s}$ over a displacement of 480 mm (one one-way sweep of the dynamic array). The circuit time of DShor with 6 QPUs to factor 2048 bit RSA integers is 297 days, which corresponds to $\tau \approx 55$ ($\sim 4.5 \times 10^4/s$ physical Bell pairs) (b) The phase diagram of DShor circuit time to factor 2048 bit RSA integers at different $j_{\max}$ and $a_{\max}$. The time is benchmarked by the circuit time of the single-core with 180 logical qubits Shor’s algorithm: $t_0 = 164.5$ days. The jerk is $j_{\max} = 30a_{\max}$. The cyan line represents the acceleration bottleneck, above which maximum speed cannot be reached due to the limit of maximum acceleration. The green line represents the speed bottleneck, the right of which the speed reaches its maximum before the acceleration reaches its maximum. The yellow dot labels the circuit time with $a_{\max} = 20\text{ m/s}^2$ and $v_{\max} = 2\text{ m/s}$ with circuit time 297 days, which corresponds to $\tau \approx 55$ ($\sim 4.5 \times 10^4/s$ physical Bell pairs). The orange star labels the circuit time with $a_{\max} = 30\text{ m/s}^2$ and $v_{\max} = 3\text{ m/s}$ with circuit time 244 days, which corresponds to $\tau \approx 40$ ($\sim 6.25 \times 10^4/s$ physical Bell pairs)

move can only generate 1875 physical 6-qubit GHZ states (which requires 9375 physical Bell pairs). Moreover, the latency between passes is long due to the acceleration/de-acceleration time of the dynamic array.

To resolve the competition between the spatial usage of the Bell pair reservoir and the inter-module bandwidth, and to reduce the delay from acceleration/de-acceleration of dynamic arrays, loading in DShor is replaced by multi-address loading as illustrated in Fig. 7. We apply a hybrid

QRAM with the first three qubits read linearly and the latter three qubits read in parallel by the Bucket-Brigade circuit [88–92]. The four input qubits are teleported to the dynamic arrays and expanded to 8 “hot encoding” address qubits. Quantum information is loaded from the address on the dynamic arrays to the data registers on the static arrays when two arrays overlap using the transversal drive-by gates. The hybrid Bucket-Brigade circuit is verified by the Shor’s simulator, and more details of multi-address loading on the dynamic array can be found in Appendix J.

The circuit time of DShor on the dynamic array is estimated by the circuit time of modular additions. The loading in one modular additions requires 4 round-trip sweeps (0.746 s each) and one Bucket-Brigade state preparation (circuit depth 663, or circuit time 0.63 s at $t_{\text{mea}} = 1\text{ms}$). The motion profile of the dynamic arrays using the assumptions mentioned above ($v_{\text{max}} = 2\text{ m/s}$, $a_{\text{max}} = 20\text{ m/s}^2$, $j = 600\text{ m/s}^3$) is shown in Fig. 8(a). The addition in the modular addition can be applied in parallel with the state preparation as shown in Fig. 6(b), so the circuit time of one modular addition is 3.62 s. In RSA 2048, there are totally $\sim 7,099,733$ modular additions, which takes 297 days, which corresponds to $\tau \approx 55$ ($\sim 4.5 \times 10^4$ physical Bell pairs between modules) as shown by the yellow dot in Fig. 8(b). At $v_{\text{max}} = 3\text{ m/s}$, $a_{\text{max}} = 30\text{ m/s}^2$, $j_{\text{max}} = 900\text{ m/s}^3$, factoring 2048 bit RSA integers needs 244.7 days ($\tau \approx 40$ or $\sim 6.25 \times 10^4$ physical Bell pairs between modules) as shown by the orange star. The compilation with multi-address therefore provides a $4\times$ bandwidth increase compared with the naive compilation of DShor on the dynamic arrays. For additional context, we assumed $\tau \approx 25$ ($\sim 10^5$ physical Bell pairs between modules) for our photonic interconnect architecture, such that the run times are within a factor of ≈ 1.56 between the two approaches. Accordingly, we conclude that the dynamic array architecture could be a viable alternative to the photonic interconnect approach.

VI. DSHOR IN THE QGPU ARCHITECTURE

With higher gate fidelities that enable drastic reduction in the code distance, we envision that DShor can be implemented with a quantum GPU (“QGPU”) architecture (≈ 100 modules connected to the shared memory). We estimate that physical error rates of $p_p \approx 10^{-5}$ will be needed to run RSA 2048 with $d = 9$ using established decoder techniques. However, we anticipate that specialized decoders that are designed with a detailed knowledge of the error channels in the hardware including erasure errors [93, 94] may enable the use of such relatively small code distances with physical error rates of $p_p \approx 10^{-4}$. Accordingly, we present a version of our DShor algorithm that is optimized around the dramatically relaxed space-like resources associated with a $d = 9$ logical encoding.

In Fig. 9(a), 20 modular processors are connected with

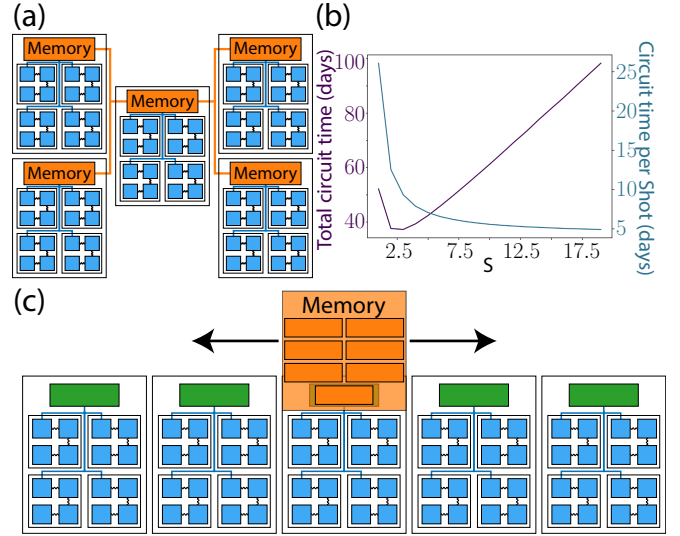


FIG. 9. **DShor in the QGPU architecture.** (a) The QGPU architecture used in DShor with photonic interconnects. Each cluster (big white box) contains one memory (orange rectangles) and 4 modular processors (small white box) with 4 QPUs (blue squares). Logical qubits in the memory is encoded in $[126, 12, 10]$ GB code, and 12 $d = 9$ surface codes are stored in the memory for the lattice surgery. The communications between the memory and the modular processors are labeled by the blue lines, where memory only needs to communicate with the router QPUs in each modular processors. The communications between the memories are labeled by the orange lines, where all memories are connected. (b) The circuit time of DShor using QGPU architecture at different s . The total circuit time (purple curve) reaches the minimum 37.3 days at $s = 3$ with 22 modular processors ($\sim 9.5 \times 10^5$ physical qubits). The circuit time per shot decreases with s , and the circuit time per shot is 4.9 days at $s = 20$. (c) The QGPU architecture with the memories connected by the dynamic arrays. Memories (orange rectangles) are teleported to the buffer memory zone (green rectangles) as the memory patch overlaps with the buffer memories.

the shared memory, and each module contains four QPUs with $8 \times 8 = 64$ logical qubits encoded in $d = 9$ surface code patches. All qubits in the memory are stored in $[126, 12, 10]$ GB codes with 12 $d = 9$ surface patches in the memory zone for the lattice surgery. The communications between the memory and modular processors are labeled by the blue lines, where each memory only needs to communicate with the router QPU in the modular processors. The communications between the memory are labeled by the orange lines, where all memory are connected. In the QGPU architecture, $N_{\text{processors}}$ modular exponentiations happen in parallel and the circuit time is reduced to $1/N_{\text{processors}}$ of its original circuit time. In Fig. 9(c), 20 modular processors are connected by the memory connected by the dynamic arrays. Memory patches stored in GB codes (orange rectangles) are teleported to the buffer memory zones (green rectangles) when the two regions overlap. Figure 9(c) shows a QGPU

architecture based on dynamic arrays.

The memory of Shor’s algorithm requires $n/2 + n/s$ qubits to store all exponents at the price of $\sim s + 1$ classical runs required. Therefore, the circuit time can be further reduced by reducing Eker’s parameter s at the price of more memory used by DShor. Fig. 9(b) shows the circuit time of DShor to factor 2048-bit RSA integers with $< 10^6$ physical qubits at different Eker’s parameter s . We assume the measurement time is 1 ms and the communication rate is 10^5 s^{-1} . The purple curve is the total circuit time $t_{\text{one shot}} \times (s + 1)$, and the blue curve represents the circuit time in one Shor’s shot. The total circuit time reaches its minimum 37.3 days at $s = 3$ with 22 modular processors ($\sim 9.5 \times 10^5$ physical qubits), and increases linearly at higher s . The circuit time per shot decreases at the higher s as expected, and the circuit time per shot is 4.9 days at $s = 20$. Therefore, it is also possible to factor 2048-bit RSA integers in 4.9 days with 21 QGPUs (21 million qubits). However, DShor in the QGPU architecture requires more frequent and complicated communications between the modules and the memory, which may become a new factor delaying the circuit time. We leave the more detailed analysis of the memory control of DShor in the QGPU architecture to future work.

VII. CONCLUDING DISCUSSION

We have presented a detailed end-to-end compilation of Shor’s algorithm that, while generalizable to any hardware platform, is specifically tailored to modular atomic quantum processors. This work serves to provide a collection and summary of the state-of-the-art algorithmic sub-routines in addition to introducing new methods that further improve the spacetime resource efficiency. These new insights include 1) modular implementation of Shor’s algorithm and the concomitant modular architecture, 2) decomposing Shor’s algorithm to fundamental operations and improved modular additions, 3) qubit re-allocations on the neutral atom platforms, 4) end-to-end simulation of Shor’s algorithm and resource estimation based on the concrete circuit. Additionally, a major contribution of this work is to present a detailed strategy for modularizing Shor’s algorithm that maximizes the compilation flexibility with respect to the buffering of communication. For the foreseeable future in which communication is more expensive than local operations, our methods for splitting the algorithm across roughly ten modules will be invaluable.

We reiterate that this work is not meant to provide a detailed resource estimate for building a quantum processor today. Rapid advances in atomic hardware, quantum error correction, and algorithm design would render such an estimate obsolete within months. On the atomic hardware side, we anticipate the possibility to reduce measurement time via, e.g., optical cavity arrays [46, 71–75]. We also anticipate the possibility to mitigate the bottle-

neck of acceleration/deceleration due to atomic inertia during transport between disparate zones through the use of *constant velocity* protocols and drive-by gates, inspired by the transportable array architecture discussed above and recently demonstrated for a low velocity of 0.05 m/s [87]. On the error correction side, we anticipate improved strategies for stabilizer measurement and classical decoding of qLDPC codes, improved strategies for code switching and lattice surgery between memory and logic, and even the possibility of transversal logic in the qLDPC code block that could obviate the need for code switching. These advances are expected to drastically improve the spacetime volume estimates, but are unlikely to eliminate the value of modular architectures in the near term.

As mentioned in the introduction, we have neglected atom loss in our compiler and resource estimates. The probability of loss during essentially all of the key primitives (initialization, cooling, one- and two-qubit gates, and slow measurement) is at the $\sim 0.1\%$ scale in state-of-the-art systems (see, e.g., refs. [55, 56, 60, 69, 95]). Therefore, in principle, the space overhead associated with loss is minimal. The time overhead is potentially more substantial because new atoms must be transported from the reservoir array [41, 42] into the memory or QPU code blocks, and because the logical encoding must be dynamic as new atoms are cycled in [96]. However, we note that our compiler can straightforwardly address this latency. As the refilling of data (ancilla) qubits cannot happen in parallel with transversal gates (QEC cycle), the latency from refilling can be included by increasing the clock time and measurement time. Finally, we note that thermal errors and atom recooling during the computation will be required, and remain largely outstanding tasks in the community. Finally, we note that it may be fruitful to design the hardware layer around atom loss, potentially by leveraging *constant velocity* operations including measurement. Such strategies might streamline atom replenishing and enable the use of fast, high-loss atom readout for stabilizer measurement and logical operations.

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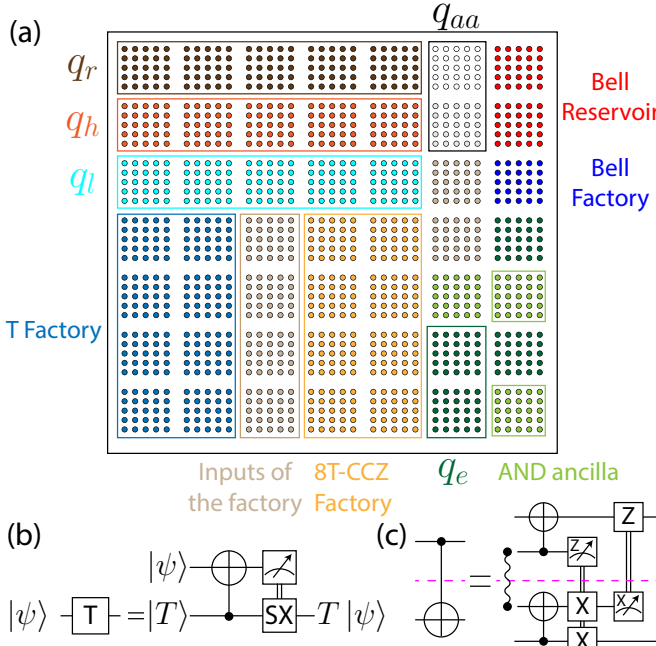


FIG. S1. **Gate time Benchmarking.** (a) The detailed qubit allocation in each QPU. q_{aa} is the antenna ancilla qubits used to generate the inter-module GHZ state, and q_r, q_h, q_l, q_e are the intermediate results as shown in Table. I. The 8T-CCZ factory on the bottom left corner of the QPU is further split to T factory, inputs of the factory and 8 ancilla qubits used in the 8T-CCZ factory. (b) The T gate is implemented by the magic state injection from the magic state $|T\rangle$ from the code cultivation. (c) The inter-module CNOTs are implemented by the gate teleportation using the inter-module Bell pairs stored in the Bell reservoir.

APPENDIX A: Gate time benchmarking

In the DShor algorithm, we use the following universal gate set: X, Y, Z, CNOT, H, S, T with the detailed implementations as follows:

- X/Y/Z: Pauli gates are ignored in the Shor's simulator as they can be pushed to the end of the circuit, which leads to the change of Pauli frames of the final measurement of Shor's algorithm [63, 64].
- CNOT: CNOT is implemented by the transversal Rydberg gates. The time of CNOT is calibrated as the clock time in this paper.
- H/S: H gate is implemented by the transversal Hadamard gates followed by the code rotation. S gate is implemented by the fold-transversal gates. As both gates only require intra-patch moving, we estimate the gate time of H/S the same as the CNOT gate [97].
- T: T gate is implemented by preparing the magic state $|T\rangle$ and injecting the magic state to the data registers as shown in Fig. S1(b). The code cultivation includes: 1. unitary encoding of ROT(3) (1

measurement), 2. ROT(3) $\rightarrow$ REG(3) (0 measurement), 3. ROT(3) $\rightarrow$ ROT(5), 4. 2 H_{XY} checks (2 measurements), 5. unitary growth to ROT(d_{fin}) (0 measurement) [98] Given the flexibility of escaping to ROT(d_{fin}), we estimates the cost of cultivating one $|T\rangle$ as $t_T = 5t_{\text{mea}}$, and we show if $t_T \leq 10t_{\text{mea}}$, the delay from the code cultivation is small in Appendix. I.

In DShor, we assume the inter-module Bell pairs can only be created in the Bell factory (the blue square), and we allocate two logical patches to store the generated inter-module Bell pairs. Inter-module logical-level CNOTs can be implemented by transversal gate teleportation which consumes d^2 physical Bell pairs (one Bell pair for each physical qubit) in the Bell pair reservoir as shown in Fig. S1(c).

APPENDIX B: Fast modular exponentiation with windowed arithmetic

Modular exponentiations are the most important sub-routines of Shor's algorithm:

$$U_g \sum_{i=0}^m |i\rangle \rightarrow \sum_{i=0}^m |i\rangle |g^i \bmod N\rangle \quad (\text{B1})$$

A naive exponentiation can use a single lookup operation to load all results to the registers [3]. Then, factoring a n -bit number using the residue arithmetic requires a lookup table with the address length n , which needs $2^n - n - 1$ Toffoli gates where Toffoli gates naturally implement. Factoring a 2048 bit RSA integer requires $\approx 3 \times 10^{616}$ Toffoli gates, which is impossible for any quantum computers under any assumptions. Therefore, the improvements on this subroutine can greatly save the spacetime volume used by Shor's algorithm.

In this section, we introduce a fast modular exponentiation protocol based on windowed arithmetic [2, 3]. Since our algorithm assumes information is encoded in two-level qubits, all quantum arithmetic is represented in the binary format instead stated otherwise (e.g. $a = \sum_k a_k 2^k$ where a_k is the k -th bit of the binary number a).

Modular exponentiations can be decomposed to modular multiplications:

$$g^i \bmod N = \left[\prod_k^n (g^{2^k i_k}) \bmod N \right] \bmod N. \quad (\text{B2})$$

The circuit of direct modular multiplications is not known, so the modular multiplication between quantum number (a) and the classical number (b) is further de-

composed to modular addition:

$$(a \times b) \bmod N = \left[\left(\sum_i^n a_i 2^i \right) \times b \right] \bmod n \quad (\text{B3})$$

$$= \left[\sum_i^n (a_i 2^i b) \bmod N \right] \bmod N. \quad (\text{B4})$$

To factor a n -bit number, we require n modular multiplications, or equivalently n^2 modular additions. Therefore, modular exponentiation requires $O(n^3)$ Toffoli gates (1 modular exponentiation $\rightarrow n$ modular multiplications $\rightarrow n^2$ modular additions $\rightarrow O(n^3)$ Toffoli gates).

The modular exponentiation can be further simplified by the windowed arithmetic by combining multiple additions/multiplications [2, 3].

$$g^i \bmod N = \left(\prod_m^n g^{2^m i_m} \bmod N \right) \bmod N \quad (\text{B5})$$

$$= \left(\prod_m^{n/w_e} g^{2^{mw_e} i_{S_m}} \bmod N \right) \bmod N, \quad (\text{B6})$$

where $i_{S_m} = i_{mw_e:(m+1)w_e}$ are the slices of i with length w_e . The modular exponentiation with the windowed arithmetic requires n/w_e multiplications, or equivalently $n/w_e(n/w_m)$ modular additions. However, each modular addition requires a lookup table with $w_e + w_m$ bit address (exact circuits in Appendix C), which needs $2^{w_e + w_m} - w_e - w_m - 1 \approx 2^{w_e + w_m}$ Toffoli gates. Therefore, modular exponentiation with windowed arithmetic requires $n/w_e(n/w_m)(n + 2^{w_e + w_m})$ Toffoli gates. The number of Toffoli gates is minimized at $w_m = w_e = O(\log(n))$, and the total number of Toffoli gates is $O(n^3/(\log(n))^3)$.

APPENDIX C: Circuit compilation of windowed arithmetic

Compilation of exponentiation with windowed arithmetic can also significantly affect the spacetime volume of Shor's algorithm [2, 3]. Our compilation is based on the compilation using lookup tables from Gidney [2, 3].

Modular exponentiation can be decomposed to modular additions from Appendix B. For simplicity, we assume all arithmetic is in the modular space of N , and the quantum modular exponentiation can be written as:

$$\sum_i |i\rangle |g^i\rangle = \sum_i |i\rangle \left| \left(\prod_m^{n/w_e} g^{2^{mw_e} i_{S_m}} \right) \right\rangle \quad (\text{C1})$$

$$= \sum_i |i\rangle \left| \left(\prod_m^{n/w_e} L_m \right) \right\rangle \quad (\text{C2})$$

where $L_m = g^{2^{mw_e} i_{S_m}}$ is a one-dimensional quantum

lookup table with the exponent $|i_{S_m}\rangle$ as the address. The multiplications can be decomposed to additions as:

$$\left(\prod_m^{n/w_e} L_m \right) \quad (\text{C3})$$

$$= P_1 \times L_1 \left(\prod_{m=2}^{n/w_e} L_m \right) \quad (\text{C4})$$

$$= \sum_a^{n/w_m} (P_1)_{S_a} L_1 2^{(a+b)w_m} \left(\prod_{m=2}^{n/w_e} L_m \right) \quad (\text{C5})$$

$$= \sum_a^{n/w_e} T_{0,S_a} \left(\prod_{m=2}^{n/w_m} L_m \right) \quad (\text{C6})$$

$$= \sum_a^{n/w_e} (P_{n/w_m-1})_{S_a} (L_{n/w_m}) \quad (\text{C7})$$

$$= \sum_a^{n/w_e} T_{n/w_m-1,S_a} \quad (\text{C8})$$

where $P_i = \prod_{m=1}^{i-1} L_m$, $P_0 = 1$, and $T_{j,a} = 2^{aw_m} (P_j)_{S_a} L_{j+1}$ is a two-dimensional quantum lookup table with two addresses: the previous product result $|P_j\rangle_{S_a}$ and L_{j+1} depending on the exponent slice $|i_{S_m}\rangle$.

As the fundamental operations of modular exponentiation are modular additions, we will first provide the circuit compilation of modular addition based on Gidney's compilation [2]. Modular additions in DShor are consist of four steps: loading, adding, wrapping and cleaning as shown in Fig. S2(e).

$$U_{add} \sum_i |i\rangle |a\rangle = \sum_i |i\rangle |a\rangle |f(i)\rangle \quad (\text{C9})$$

$$= \sum_i |i\rangle |[a + f(i)] \bmod N\rangle \quad (\text{C10})$$

The first line is to load the classical information $f(i)$ into buffer qubits, where $f(i)$ is the tables value associated with the quantum address $|i\rangle$. In the compilation of DShor, we prefer to reduce time cost at the expense of space cost, so the values are loaded by sequential QRAM as shown in Fig. S2(c, d). We also provide the compilation of modular additions with multi-address QRAM on the dynamic array in Appendix J, which can also be applied on other architectures. The first two modular multiplications are replaced by direct loadings as shown in Fig. S2 [99].

Since all additions are in the modular space of N , instead of decomposing modular additions to three or five direct additions, we introduce a wrapping step to decompose the modular addition with two modular additions at the price of one additional overflow qubit [2, 3, 100–103].

Assume that the added number has f bits plus 1 overflow bit (total $f + 1$ bits). To perform the wrapping, we replace all table values in the additions in the modular

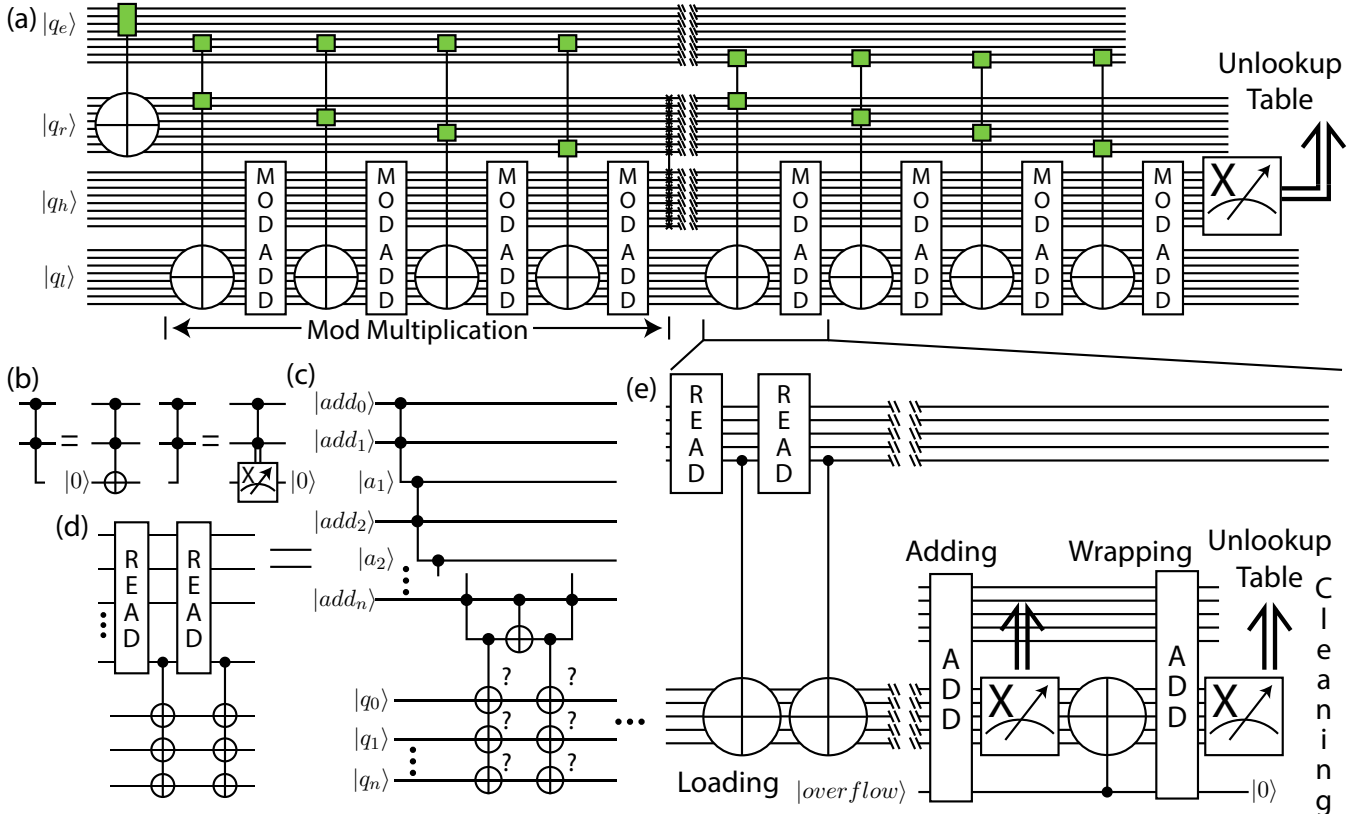


FIG. S2. **Modular exponentiations in DShor.** (a) The modular exponentiations can be decomposed to loadings and modular additions. The addresses of loadings are represented by the light green squares. The first two modular multiplications are applied by direct loadings. (c) The circuit of unary loadings used in DShor with the logical AND and UNAND gates in (b). (d) For illustration, we simplify the cascades of AND and UNAND gates between loadings as read gates. (e) The detailed circuit of modular additions. Classical tables are loaded to $|q_l\rangle$ followed by the direct additions. $|q_l\rangle$ is cleaned by the transversal X-measurement, and the measurement result is recorded to generate the unlookup table. Another loading controlled by the overflow qubit $|q_o\rangle$ is loaded to the $|q_l\rangle$ followed by another direct addition to wrap the addition result. $|q_l\rangle$ is again cleaned by X-measurement. These two unlookup tables are merged during the un-exponentiations.

space of N to:

$$|i\rangle |a + f(i) \bmod N\rangle \rightarrow |i\rangle |a + f(i) - N + 2^f\rangle \quad (\text{C11})$$

If $a + f(i) \geq N$, $a + f(i) - N + 2^f \geq 2^f$ and the overflow bit $|q_o\rangle$ must be 1. Otherwise, $a + f(i) - N + 2^f < 2^f$ and the overflow must be 0. Therefore, we can determine if a “wrapping” should happen during the addition and apply it by a single address lookup table $\{0 : 2^f + N, 1 : 2^f\}$, or equivalently a cascade of CNOTs shown in Fig. S2(e):

$$\begin{aligned} & |i\rangle |a + f(i) - N + 2^f\rangle \\ &= |i\rangle |a + f(i) - N + 2^f, q_o = 1\rangle \quad (a + f(i) > N) \\ &+ |i\rangle |a + f(i) - N + 2^f, q_o = 0\rangle \quad (a + f(i) < N) \\ &\rightarrow |i\rangle |a + f(i) - N + 2^{f+1}, q_o = 1\rangle \\ &+ |i\rangle |a + f(i) - N + 2^{f+1} + N, q_o = 0\rangle \\ &= |i\rangle |a + f(i) - N\rangle \quad (a + f(i) > N) \\ &+ |i\rangle |a + f(i)\rangle \quad (a + f(i) < N) \end{aligned} \quad (\text{C12})$$

One trick we apply here is that the direct addition with $f + 1$ bits is implicitly in the modular space of 2^{f+1} . Therefore, 2^{f+1} is 0 in the direct addition.

The quantum information in the buffer qubits $|q_l\rangle$ is cleaned by a transversal X-basis measurement after the addition as shown in Fig. S2(e):

$$|i\rangle |a + f(i)\rangle |f(i)\rangle \rightarrow (-1)^{f(i) \wedge M} |i\rangle |a + f(i)\rangle \quad (\text{C13})$$

where M is the measurement result. The cleaning of phase errors is combined with other memory cleaning in the Shor’s algorithm shown in Appendix G.

APPENDIX D: Shor’s algorithm with approximate residue arithmetic

Shor’s algorithm with approximate residue arithmetic significantly reduces the qubit used by Shor’s algorithm but with longer run time. In this section, we will focus on how to decompose the modular exponentiations of a huge number into multiple modular exponentiations of small

numbers with residue arithmetic [2]. In our resource estimation, we assume the number to be factored are RSA numbers and use Ekerå's Shor's algorithm using discrete short logarithms [4]. We also use masked qubits when accumulating the modular exponentiation results of each residue system to reduce the qubit used, which leads to a blurred measurement result of the Shor's algorithm in the frequency basis [2].

All variants of Shor's algorithm require $g^e \bmod N$ over certain superpositions of e , which requires $O(n)$ qubits to store all intermediate results of modular exponentiation mentioned in Appendix C [3]. However, using the residue arithmetic, the qubits used to store all intermediate results can be significantly reduced to $O(\log(n))$.

From the Chinese Remainder Theorem, given the series of a_i and p_i where $x = a_i \bmod N$, if all p_i are coprime, there exists a unique solution of x

$$x \bmod P = \sum_i a_i P_i r_i \quad (D1)$$

where $P_i = \prod_{j \neq i} p_j$ and $r_i = P_i^{-1} \bmod p_i$. The intermediate results stored have size $|p_i|$ instead of n . Therefore, in the Shor's algorithm, if all $a_i = g^e \bmod p_i$ are found, $\prod p_i = N$ and p_i are coprime, and g^e can be reconstructed with small numbers from Eq. D1. However, finding all p_i is harder than factoring N . To find the residue system without factoring N , we take a redundant module of g^e :

$$\sum_{e=0}^{2^m-1} |e\rangle |g^e \bmod N\rangle = \sum_{e=0}^{2^m-1} |e\rangle |g^e \bmod L \bmod N\rangle \quad (D2)$$

where $L \geq N^{2^m} \geq g^e$. If we can find all coprime p_i with $\prod p_i = L$, this could form the residue system for $g^e \bmod N$. In the Shor's algorithm, L and p_i are found by finding the series of p_i with $\prod p_i = L \geq N^{2^m/w_1}$. More details about the requirement of residue system can be found in Gidney's approach to Shor's algorithm [2].

As mentioned in Appendix C, the modular exponentiation can be decomposed to modular multiplications $g^e = \prod_k g^{2^k e_k} = \prod_k L_k$. With the residue arithmetic, since all modules in the residue system are small, the modular multiplications can be replaced with modular additions heuristically. The generator g_{p_i} of p_i can be found by the brute force search, the exponent $D_{i,k}$ giving $g_i^{D_{i,k}} = L_k \bmod p_i$ can be found, and the modular multiplications can be replaced by modular additions

$$g^e \bmod p_i = g_{p_i}^{S_i} \bmod p_i \quad S_i = \sum_k D_{i,k} e_k \quad (D3)$$

Since g_{p_i} is the generator of p_i , it has order $p_i - 1$, which gives $g_{p_i}^{S_i} = g_{p_i}^{S_i \bmod (p_i-1)}$. With all $g^e \bmod p_i$ found, $g^e \bmod N$ can be found by Eq. D1.

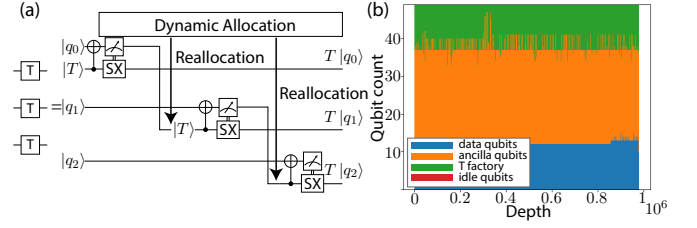


FIG. S3. **Qubit re-allocation in DShor.** DShor will mark all idle qubits and re-allocate them when the Shor's simulator asks for a new qubit. The minimum illustration of qubit re-allocation is in (a). Three T gates can be implemented with only one ancilla qubits by reusing the measured qubits after the magic state injection. (b) The qubit allocation in DShor during the modular exponentiation. DShor will allocate qubits between the T factory and the cache (ancilla qubits) to reduce the spacetime volume of Shor's algorithm.

APPENDIX E: Distributed modular addition in DShor

In the DShor, all qubits storing exponents ($Q_{exponent}$) and final results (Q_{acc}) are stored in the memory. The qubits in the memory will only be accessed once in each modular exponentiation (700 s in the single-module Shor's algorithm). The other qubits actively used during modular exponentiation are distributed evenly through all QPUs as shown in Table I.

The naive compilation of Shor's algorithm on a modular quantum computer requires $|p|$ inter-module CNOTs controlled by the control qubit (the green register) as shown in Fig. S4. To reduce inter-module communications, we use one GHZ state to pre-connect all modules, and the table values are loaded by broadcasting the controlled qubit to all qubits in the GHZ state [7]. This reduces the number of inter-module CNOTs per loading from $|p| - |p|/N_{QPU}$ to N_{QPU} , and the burden of inter-module communications is evenly distributed to all QPUs. The modular lookup table can reduce inter-module connections if $N_{QPU} < \frac{1}{2}\sqrt{|p|^2 - 4|p|} + |p|/2 \approx |p|$. Therefore, DShor at least requires 2 qubits of each category per QPU. In RSA 2048, $|p| = 24$ and DShor can be distributed to at most 12 QPUs.

The 8T-CCX factory also requires intensive inter-module communications if the control qubits and the target qubit are not in the same QPU. During the address reading of the quantum lookup table, the address qubits are teleported to ensure that all AND and UNAND gates are applied within one QPU as shown in Fig. S4(b). A similar technique is used in the addition ladders [76]. Cleanings are implemented during the un-exponentiations, and the cleanings of phase errors can be simplified to quantum loadings with only one target [2, 3]. To further reduce the cost of cleaning, we split a n -qubit address in the cleaning to two $n/2$ "hot encoding" addresses [2, 3]. After decomposing cleanings to loadings, the distribution of cleanings is the same as the

distribution of loadings.

APPENDIX F: Qubit Reallocation

Since atoms can be flexibly rearranged on the neutral atom platform, all measured (clean) qubits are marked as idle (except some intermediate results during the modular exponentiations, such as q_h). Instead of requiring more qubits in total when one subroutine asks for more qubits, QPUs will first re-allocate the idle qubits. One simple example of qubit reallocation is illustrated in Fig. S3(a), where 3 T gates can be injected with only 1 ancilla qubit but with triple circuit depth. In DShor, most reallocations happen between the qubits in 8T-CCX factory and those in caches as shown in Fig. S3(b). This reallocation can increase the parallelism in each QPU and further reduce the spacetime volume of DShor.

APPENDIX G: Verification of DShor

Verifying the circuit of modular exponentiation in Appendix C is too computationally challenging for the quantum circuit simulation packages (e.g. Qiskit), since they track all components in the Hilbert space. For example, according to Table I, modular exponentiation in the 2048-bit RSA integers requires at least 99 qubits, which requires at least $2^{99} \approx 10^{30}$ 99-bit numbers to exactly simulate the circuit, which is beyond the capability of classical computation.

To efficiently verify our modular exponentiations and the corresponding circuits, we design an algorithm that only tracks very few samples in the Hilbert space. We focus on the modular exponentiation used in RSA 2048 as an example to explain our verification:

$$\sum_e |e\rangle \rightarrow \sum_e |e\rangle |g^e \bmod N\rangle$$

For simplicity, we will only track one single Hilbert trajectory in the modular exponentiation: $|e = \tilde{e}\rangle$. The initial two multiplications of modular exponentiation is applied by direct loading result to q_r :

$$|\tilde{e}\rangle \rightarrow |\tilde{e}\rangle |g^{\tilde{e}0:2w_1}\rangle_{q_r} |0\rangle_{q_h}$$

$T_{2,0}$ is loaded to $|q_l\rangle$ and added to $|q_h\rangle$:

$$|\tilde{e}\rangle \rightarrow |\tilde{e}\rangle |g^{\tilde{e}0:2w_1}\rangle_{q_r} |T_{2,0}(0, \tilde{e}S_2)\rangle_{q_h} |T_{2,0}(0, \tilde{e}S_2)\rangle_{q_l}$$

$|q_l\rangle$ are cleaned by the transversal X measurement, reset to $|0\rangle$, and the measurement result M_0 is recorded:

$$(-1)^{M_0 \& T_{2,0}(0, \tilde{e}S_2)} |\tilde{e}\rangle \rightarrow |\tilde{e}\rangle |g^{\tilde{e}0:2w_1}\rangle_{q_r} |T_{2,0}(0, \tilde{e}S_2)\rangle_{q_h} |0\rangle_{q_l}$$

The negative phase is corrected during the modular un-exponentiation. All tables of $T_{2,k}$ are loaded in the same

way, and all measurement results are recorded as M_k . The final state is:

$$|\psi\rangle = (-1)^{\sum_k M_k \& T_{2,k}(0, \tilde{e}S_2)} |\tilde{e}\rangle |g^{\tilde{e}0:2w_1}\rangle_{q_r} |P_3\rangle_{q_h} |0\rangle_{q_l}$$

Here we use the fact that $\sum_k T_{2,k} = \sum_k 2^{kw_m} (P_2)_{S_k} L_2 = P_2 \times L_2 = P_3$. $|q_r\rangle$ and $|q_h\rangle$ are swapped, and $|q_h\rangle$ is cleaned by transversal X measurement. The measurement result is recorded as $\tilde{M}_2$

$$|\psi\rangle = (-1)^{P_2 \& \tilde{M}_2 + \sum_k M_k \& T_{2,k}(0, \tilde{e}S_2)} |\tilde{e}\rangle |P_3\rangle_{q_r} |0\rangle_{q_h} |0\rangle_{q_l}$$

This loop is repeated with all $T_{j,:}$, and the final state is:

$$|\psi\rangle = (-1)^\phi |\tilde{e}\rangle |g^{\tilde{e}}\rangle_{q_r} |0\rangle_{q_h} |0\rangle_{q_l}$$

where ϕ depends on all measurement results of qubit cleaning. The un-exponentiation is applied by running the exponentiation inversely with phase-up cleaning at each loop [2].

To simulate the RSA 2048 challenge, we start with 2^5 random 24-bit $|\tilde{e}\rangle$ and 3 group of $|0\rangle^{\otimes 25}$ for $|q_r\rangle$, $|q_h\rangle$ and $|q_l\rangle$. As shown in Fig. S4, each addition is split to loading, adding, wrapping, and cleaning. Each Hilbert trajectory of $|\tilde{e}\rangle$ is updated at each of these four steps similarly with the example shown above. All measurement results are recorded and used in the modular un-exponentiation. At the same time, each time the modular addition happens, a circuit of modular addition will be applied on the corresponding quantum registers. Therefore, the parallel evolution of the quantum circuit and the back-end Hilbert trajectory guarantees the consistency between the algorithm and the circuit. We collect all qubit usage and estimate the circuit depth and qubits used from the circuit evolved during the Shor's algorithm.

More details about the estimation methods of the Shor's simulator can be found in Appendix H.

APPENDIX H: Estimation methods in DShor

In this section, we will present the simulation procedures and the memory-QPU interactions in the DShor simulator. In the DShor, $|Q_e\rangle$ and $|Q_{acc}\rangle$ are stored in the memory, and the Shor's algorithm can be decomposed to 4 steps as illustrated in Fig. 2. When loading the short logarithms $|q_e\rangle$ to the QPU, we simplify the iteration over all qubits in $|Q_e\rangle$ with window size w_1 to the iteration over the same w_1 qubits for $\text{ceil}(m/w_1)$ times as shown in Fig. S5(a-c) without losing generality. In DShor, we search the parameter space over $w_1 = 2 - 8$ and fix $w_1 = 6$ for the minimal circuit time as shown in Fig. S6(b). Buffer qubits (green squares) read 6 qubits in the memory and are teleported from the memory to the router QPU (Fig. S5(a)), and the short logarithm is loaded from the buffer qubits (Fig. S5(b)). Buffer qubits are teleported back to the memory after the current short logarithm is loaded to $|q_e\rangle$. During the loading, the other 6 buffer qubits in the memory will read the next 6 qubits

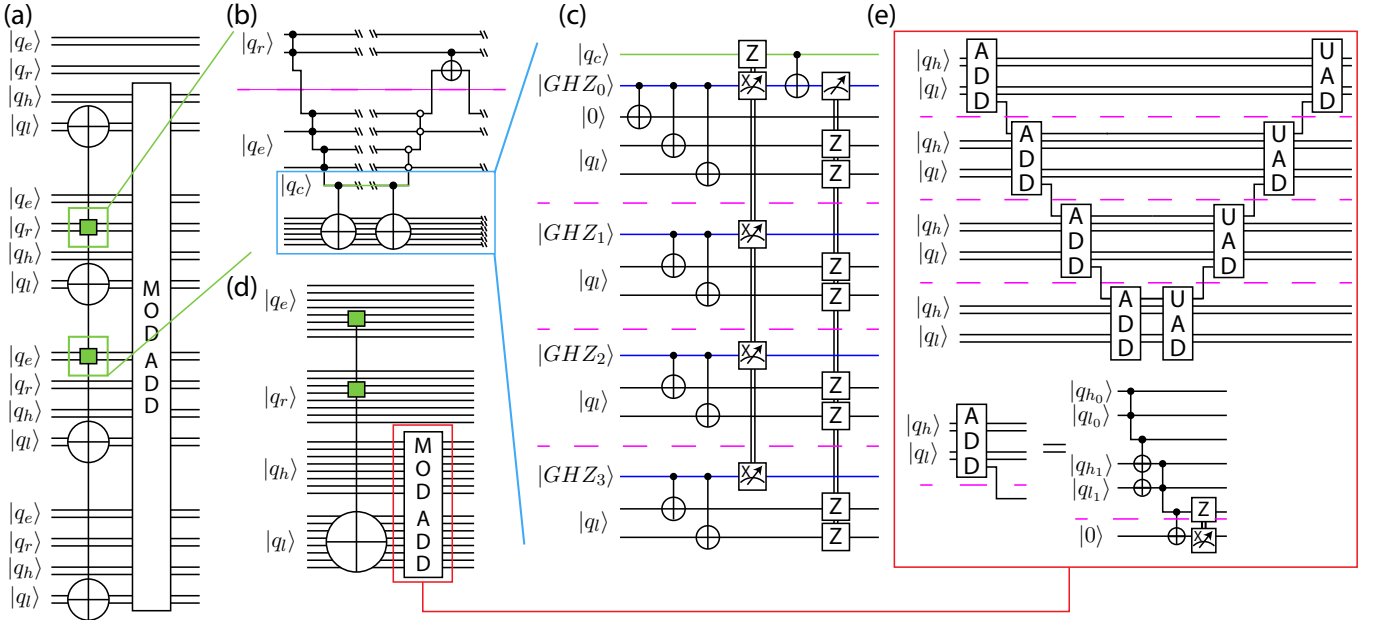


FIG. S4. **Detailed circuit of distributed modular loadings/additions.** (a-c) The detailed circuit of modular loadings. The green squares are addresses. The naive circuit of loadings in (a) is illustrated in (b), where addresses are accessed sequentially. The qubit recording the result of the memory reading $|q_c\rangle$ is labeled by the green line. In the modular loadings, all addresses are teleported to the same QPU to avoid the intense communications in the 8T-CCX factory. The cascade of CNOTs in the blue box are split in to multiple pre-loadings as illustrated in (c). The reading results $|q_c\rangle$ is teleported to all QPU through qubits in one GHZ state. The modular addition in (d) can be distributed with nearest-neighbor communications as illustrated in (e). The purple lines label the boundary of each QPU. The overflow qubits are teleported to the neighbor QPU during the addition ladder, and teleported back to the original QPU during the un-addition ladder.

from $|Q_e\rangle$ as shown in Fig. S5(c). We assume that buffer qubits can read information from the memory before the short logarithm is loaded to $|q_e\rangle$ (74.5 s in the 6 QPU DShor). As we estimate the iteration over $|Q_e\rangle$ to iterate w_1 qubits for m/w_1 times, Shor's simulator will not check the Hilbert trajectory when loading short logarithm to the QPU, and replace the table value S_{p_i} to a random table as shown in Fig. S5(b). To further reduce the computation resource used by the simulator, we only iterate the loading 40 times and record the circuit time t_{avg} , and the circuit time of m/w_1 loadings is estimated by $t_{avg} \times \text{ceil}(m/w_1)$. When the $|q_e\rangle$ is compressed to $|p_i - 1|$ bits, Shor's simulator will initialize 32 Hilbert trajectories with random $|q_e\rangle$, and the Shor's simulator will verify if all Hilbert trajectories are $|q_e \bmod (p_i - 1)\rangle$ at the end of the circuit as shown in Fig. S5.

During the modular exponentiation, Shor's simulator will track 32 Hilbert trajectories with random $|q_e\rangle$. g^e is calculated to $|q_r\rangle$ by decomposing the modular exponentiations to the fundamental operations as discussed in Section III A and Appendix C, E, and G, and the Shor's simulator will update all Hilbert trajectories after each fundamental operations and record all measurement results for the delayed phase cleaning. At the end of the modular exponentiation, the Shor's simulator will verify if all Hilbert trajectories are $|e\rangle_{q_e} |g^e \bmod p_i\rangle_{q_r}$, but ignore all phase errors. $|Q_{acc}\rangle$ is teleported from the memory to

the QPU, and $r_i u_i$ is loaded to $|Q_{acc}\rangle$ based on $|q_r\rangle$ as shown in Fig. S5(g). As the prime systems are different in different RSA challenges and N , we replace $r_i u_i$ to a random table for simplicity. $|Q_{acc}\rangle$ is then teleported back to the memory in Fig. S5(g). Shor's simulator will decompose $-g^e \bmod p_i$ and memory cleaning to fundamental operations as shown Fig. S5(h) [2, 3, 104], and Shor's simulator will verify if $|q_r = 0\rangle$ without phase errors in all Hilbert trajectories as shown in Fig. S5(h) and record the circuit time t_{p_i} to iterate one p_i in the prime system. The final circuit time of one shot in DShor is estimated by $t_f = t_{p_i} \times nm / (w_1 |q_e|)$. The circuit time for the inverse Quantum Fourier transformation measurement is ignored as it is negligible compared with the circuit time of the modular exponentiations [2, 105–110].

APPENDIX I: Investigations of more parameters in the DShor

In the main text, we focus on the DShor with 6 QPU at $t_{mea} = 1$ ms as shown in Fig. 5(a) with $w_1 = 6$, $w_e = w_m = 3$, $t_T = 5t_{mea}$ and $s = 8$. In this section, we will discuss the influence of other parameters in the DShor as shown in Fig. S6.

In Fig. S6(a), we estimate the circuit time of DShor with 6 QPUs at measurement time $t_{mea} = 250 \mu s$. The time is calibrated by the single-module DShor with 180

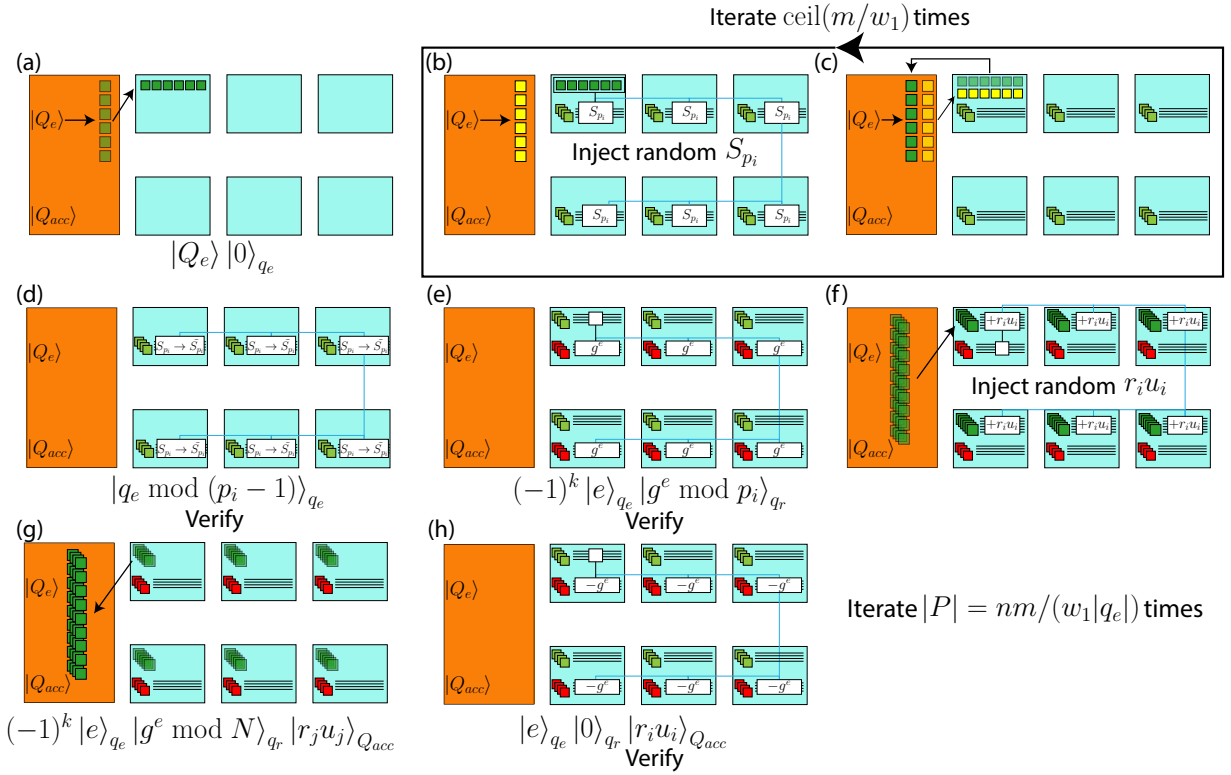


FIG. S5. **Estimation method in DShor.** (a-c) Iteration over all qubits of $|Q_e\rangle$ is estimated by iterating w_1 qubits from $|Q_e\rangle$ for $\text{ceil}(m/w_1)$ times. The Shor’s simulator will simulate 40 loadings, record the circuit time, and calculate the average circuit time for one iteration (t_{avg}). The circuit time of $\text{ceil}(m/w_1)$ iterations is estimated by $t_{\text{avg}} \times \text{ceil}(m/w_1)$. (a) 6 buffer qubits are teleported from the memory to the QPUs, (b) and S_{p_i} is loaded to $|q_e\rangle$. (c) Buffer qubits will be teleported back the memory when the loading is finished. (d) Shor’s simulator will track 32 Hilbert trajectories with random q_e and verify if all the trajectories are compressed to $|q_e \bmod (p_i - 1)\rangle$ at the end of the compression. (e) Shor’s simulator will track 32 Hilbert trajectories with random q_e during the modular exponentiation and verify if all Hilbert trajectories are $(-1)^k |e\rangle_{q_e} |g^e \bmod N\rangle_{q_r}$. (f) The accumulator $|Q_{\text{acc}}\rangle$ is teleported to QPUs and records the result of the modular exponentiation $|q_r\rangle$. (g) The accumulator $|Q_{\text{acc}}\rangle$ is teleported back to the memory. (h) $|q_r\rangle$ will be cleaned and the Shor’s simulator will verify if all trajectories have $|q_r = 0\rangle$ without phase errors and will record the circuit time t_{p_i} as the circuit time to iterate one p_i in the prime system. The circuit time of one shot in the Shor’s algorithm is estimated as $t_{p_i} \times nm/(|q_e|w_1)$.

qubits (excluding memory): $t_0 = 65.2$ days. DShor still shows small advantages when the communication cost is low $\tau \leq 3$ ($\geq 8.3 \times 10^6 s^{-1}$ communications), and the modularization of DShor with 6 QPUs is “free” when $\tau \approx 3$, which is much smaller than the “free modularization” threshold when $t_{\text{mea}} = 1$ ms. The delay of inter-module communications is more significant when $t_{\text{mea}} = 250 \mu s$ since fewer communications can be hidden behind the measurements. The overhead from communications of the DShor with 6 QPUs at $\tau = 25$ ($10^5/s$ physical Bell pairs) is 200%. However, the circuit time of DShor with $t_{\text{mea}} = 250 \mu s$ is still 20% – 100% faster than that with $t_{\text{mea}} = 1$ ms depending on the communication cost for $\tau = 1$ to 40. We also measure DShor with 6 QPUs at different code distances and measurement times in Fig. S6(b). The boundary of “free modularization” is also shifted to lower code distance as shorter measurement time allows less parallelism between the inter-module communications and intra-module operations.

In Section IV, we fix $s = 8$, $w_m = w_e = 3$, and $w_1 = 6$.

As the qubits required during the dephasing will increase exponentially with w_m and w_e , we fix $w_e = w_m = 3$. w_1 is the window size used when loading the short logarithms from the memory. In Fig. S6, we change $w_1 = 2 - 10$ in the DShor with 6 QPUs at $t_{\text{mea}} = 1$ ms, and the circuit time of DShor reaches the minimum at $w_1 = 6$, which becomes the canonical choice of w_1 in the main text.

In Appendix. A, we assume the time of code cultivation $t_T = 5t_{\text{mea}}$. The time of code cultivation can change significantly depends on the target logical error, quantum error correction codes used in the code cultivation, and the techniques used in the code changing. In Fig. S6, we change the cost of code cultivation from t_{mea} to $20t_{\text{mea}}$, and the delay from the code cultivation is ignorable ($\leq 5\%$) if $t_T \leq 10t_{\text{mea}} = 10$ ms as the code cultivation can happen in parallel with the ladders of CNOTs in the 8T-CCX factory.

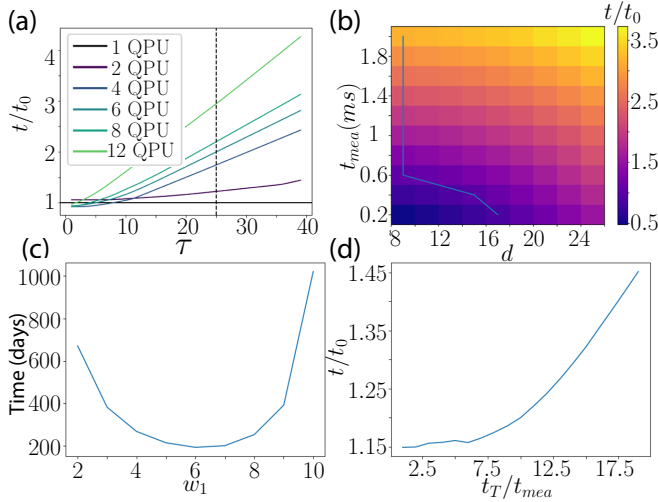


FIG. S6. **DShor with more parameters.** (a-b) We estimate the space and time usage of the DShor with 2, 4, 6, 8, 12 QPUs to factor RSA 2048-bit integers. The circuit time is benchmarked by the circuit time of single-core Shor’s algorithm with 180 qubits with $t_{mea} = 250 \mu s$: $t_0 = 65.2$ days. (a) The circuit time of DShor with 2, 4, 6, 8, 12 QPUs at different costs of inter-module communications, where the communication cost is benchmarked by the cost of logical intra-module CNOTs (without QEC) time: $\tau = \frac{t_{inter}}{t_{intra}}$ and $t_{intra} = 250 \mu s$. $\tau = 25$ corresponds to 10^5 physical inter-module Bell pairs generated per second as labeled by the dashed black line. DShor gains small advantage at low communication cost, and the delay from the inter-module communications is much more significant compared with DShor with $t_{mea} = 1$ ms as fewer operations can be hidden behind the measurements. The circuit time of 6-QPU DShor with communication rate 10^5 Bell pairs/sec is $\sim 100\%$ longer than the single-module Shor. (b) The circuit time of DShor with 6 QPUs at different code distances and measurement times. The boundary of “free modularization” is shifted to lower code distances as fewer operations can happen in parallel with the measurements. (c) The circuit time of DShor with 6 QPUs and $t_{mea} = 1$ ms at different w_1 . The circuit time reaches the minimum at $w_1 = 6$, which becomes the canonical w_1 in the main text. (d) The circuit time of DShor with 6 QPUs and $t_{mea} = 1$ ms at t_T from t_{mea} to $20t_{mea}$. The delay from code cultivation is ignorable when $t_T < 5t_{mea}$, and the delay is $\leq 5\%$ when $t_T \leq 10t_{mea}$ as code cultivation can happen in parallel with the ladders of CNOTs in the 8T-CCX factory.

APPENDIX J: Multi-address loading on the dynamic array architecture

Apart from the compilation of DShor on the static arrays with photonic inter-module connection, we provide the compilation of DShor on the arrays connected by the dynamic arrays as illustrated in Fig. 6(a).

To provide a direct comparison with the photonic connected platforms, we focus our compilation on seven static arrays connected by four dynamic arrays. We assume both static array and dynamic arrays have dimension 2 mm^2 with 7×7 logical qubits as illustrated in

Fig. 1. The range of movement of dynamic array can cover all static arrays as illustrated in Fig. 6 but can only move collectively. We assume dynamic arrays can move with the acceleration $a_{max} = 20 \text{ m/s}^2$, maximum speed $v_{max} = 2 \text{ m/s}$ and jerk $j = 600 \text{ m/s}^3$.

As discussed in Section V, to resolve the competition between the spatial usage of the Bell pair reservoir and the inter-module bandwidth, we provide a special compilation of DShor using multi-address loading as illustrated in Fig. 7 with more details in Fig. S9. We applied a hybrid QRAM with first three qubits read linearly and the latter three qubits read in parallel by the Bucket-Brigade circuit [88–92].

Fig. 7 shows the circuit gadget used in the modular loading on the dynamic array. The latter three address qubits (dark green boxes) and the input qubit (light green boxes) from the linear read are teleported to the first dynamic array. The Bucket-Brigade circuit will expand the three address qubits into eight one-hot encoding qubits (yellow boxes). Four encoded qubits are teleported to the second dynamic array. The address and input qubits are “duplicated” by maximally entangling them with four ancilla qubits, and the same procedures are repeated on the third and fourth dynamic arrays. The dynamic array will carry the “one-hot” encoding qubits and the antenna qubits (light blue boxes) for Bell pair (dark blue boxes) generations to static arrays. When the dynamic array overlaps with the static array, inter-module CNOTs will be applied by the drive by gates. An example of GHZ state preparation by drive-by gates is illustrated in Fig. 7(b). To maximally use the bandwidth of the dynamic array, half of the table values are loaded on the buffer qubits and later loaded back to the q_i . Therefore, one cascade of CNOTs can be split into two, and the loading can be finished within one sweep.

A more detailed protocol is shown in Fig. S9. Before the transverse move of the dynamic array, the three address qubits are expanded to eight one-hot encoding qubits on the first dynamic array, and half of the qubits are teleported to the second dynamic array (Fig. S9(a)). The same procedure happens to the third and fourth dynamic arrays. Then, the dynamic arrays sweep through the static array. We assume the static and dynamic arrays are overlapped by a 7×2 logical qubit zone. Table values are loaded to the 5×2 qubit zone, and the 2×2 qubit zone stores the Bell pairs generated by drive-by gates. During the forward sweep, four table values are loaded to the quantum registers, and each module generates two inter-module Bell pairs with each neighbor modules (Fig. S9(b)). During the backward sweep, the remaining four table values are loaded, one GHZ state across modules is generated, three quantum addresses used in Bucket-Brigade are teleported to the dynamic array (Fig. S9(c,d)), and all necessary inter-module Bell pairs between dynamic arrays are generated (Fig. S9(e)). The Bell pairs between the dynamic arrays are generated using the ancilla qubits on the static array (light blue squares), and the Bell pairs generated by the ancilla

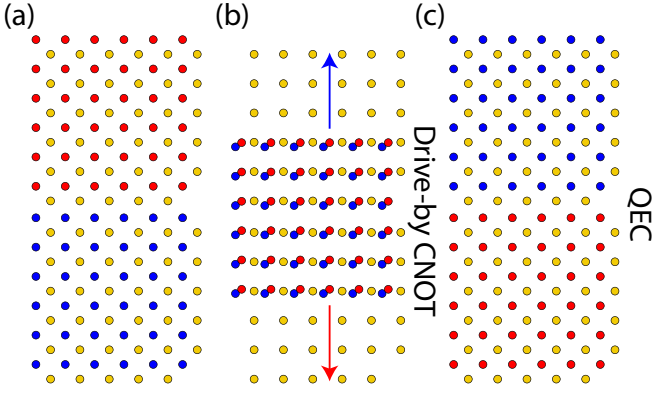


FIG. S7. **Swap CNOT.** In the machine code of the DShor, we assume the logical CNOT is applied by swapping the positions of two logical patches. (a-b) Two logical patches are moving toward each other, and the drive-by CNOTs are applied when two data qubit patches overlap. (c) Two patches swap their position and use the QEC ancilla qubits (yellow qubits) for the following QEC cycle.

qubits share the same label in the square (e.g. the Bell pairs with label “+” are generated by the ancilla qubits with label “+”) as shown in Fig. S9(f). After four transverse sweeps, all static arrays will use the two nearest-neighbor Bell pairs and one GHZ states across arrays for modular addition as shown in Appendix E.

APPENDIX K: Machine code in DShor

We also present the exact moving of atoms in the logical AND gates in DShor as shown in Fig. S8, and the video of the atom moving is in the supplementary material. We assume the logical CNOTs are implemented by the “swap” logical CNOTs as shown in Fig. S7. Instead of moving one patch close to another patch, we assume two patches are moving in opposite directions and swap their positions. A transversal drive-by CNOT is implemented when two patches overlap followed by QEC cycles after two patches swap their positions. We roughly estimate the circuit time in Fig. S8 is 31.5 ms, which is 26% longer than the circuit time simulated in the Shor’s simulator since we assume all logical CNOTs share the same clock rate regardless of the moving distance, and some parallel operations on the circuit become sequential due to the moving constraints. However, we expect that the measurement time is the dominant factor in the CCX factory, and the latency from moving distance/structure is less significant. Our moving strategy is not optimal, and the 26% overhead is an overestimate of the exact circuit time of the CCX factory. The exact moving of atoms can change significantly under different hardware assumptions. We will leave the optimization of atom transport in Shor’s algorithm to future work.

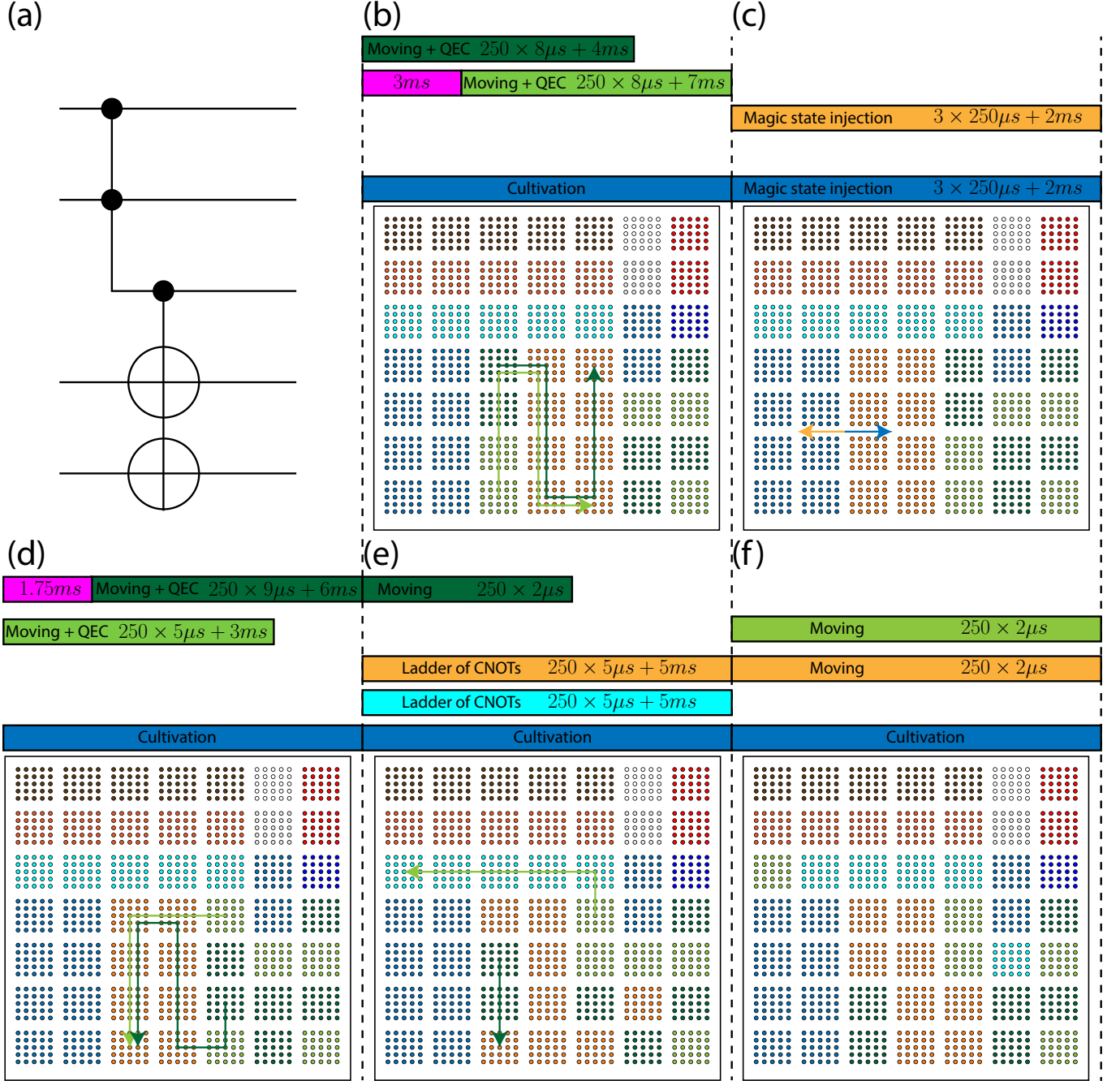


FIG. S8. **Atom moving of the logical AND gate in DShor** The machine code of loadings circuit shown in (a). The color bar on the top indicates the time spent by qubits with the same color. The pink bar suggests the idle time of qubits. The arrows label the movement of atoms, and at most two movements are labeled in each step for illustration. (b) The ladder of CNOTs in the 8T-CCX factory. (c) T gate is injected to the ancilla qubits in the factory from magic state $|T\rangle$. (d) Ladder of CNOTs to un-entangle the ancilla qubits and data qubits in the factory. (e) Classical information is loaded from the control qubit $|q_c\rangle$ to the buffer qubits $|q_r\rangle$. (f) Atoms are rearranged for the next loading gate.

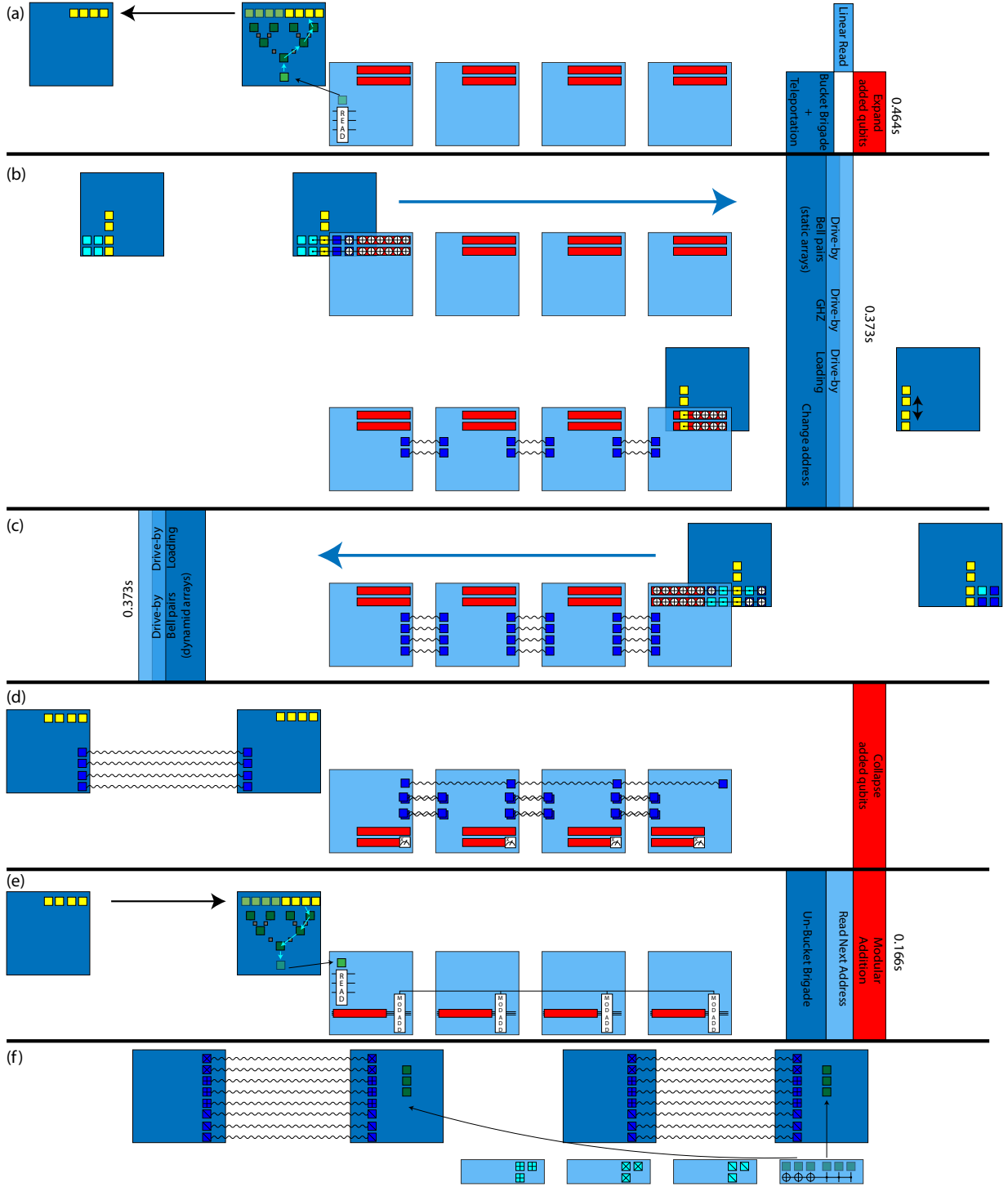


FIG. S9. **Machine code of modular loadings using the dynamic array.** The color bars on the sides indicate the time spent by the qubits with the same color. We illustrate the most complicated sweeps (the last sweep involving additions) during the modular addition. (a) Before the transverse move of the dynamic array, the three address qubits are expanded to eight one-hot encoding qubits on the first dynamic array, and half qubits are teleported to the second dynamic array. (b) Four table values are loaded to the quantum registers, and each module generate two inter-module Bell pairs with each neighbor modules during the forward sweep. (c) During the backward sweep, the remaining four tables values are loaded, one GHZ state across modules is generated, the three quantum addresses used in Bucket-Brigade are teleported to the dynamic array, and all necessary inter-module Bell pairs between dynamic arrays are generated. (d) The entanglement structure in the dynamic arrays and static arrays after one round-trip sweep. Static arrays will use 2 nearest neighbor Bell pairs and one GHZ state for the modular addition. (e) “Hot encoding” addresses are restored to original addresses by the un-Bucket-Brigade circuit. (f) The entanglement structure between the dynamic arrays. The Bell pairs are generated by the ancilla qubits (light blue squares) with the same labels on the static arrays. For example, the Bell pairs with the label “+” are generated by the ancilla qubits with the label “+”.

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