

# Space-Efficient Quantum Algorithm for Elliptic Curve Discrete Logarithms with Resource Estimation

Han Luo<sup>\*1</sup>, Ziyi Yang<sup>\*2,3</sup>, Ziruo Wang<sup>2,3</sup>, Yuexin Su<sup>2,3</sup>, and Tongyang Li<sup>†2,3</sup>

<sup>1</sup>Interdisciplinary Information Sciences, Tsinghua University

<sup>2</sup>Center on Frontiers of Computing Studies, Peking University

<sup>3</sup>School of Computer Science, Peking University

## Abstract

Solving the Elliptic Curve Discrete Logarithm Problem (ECDLP) is critical for evaluating the quantum security of widely deployed elliptic-curve cryptosystems. Consequently, minimizing the number of logical qubits required to execute this algorithm is a key object. In implementations of Shor's algorithm, the space complexity is largely dictated by the modular inversion operation during point addition. Starting from the extended Euclidean algorithm (EEA), we refine the register-sharing method of Proos and Zalka and propose a space-efficient reversible modular inversion algorithm. We use length registers together with location-controlled arithmetic to store the intermediate variables in a compact form throughout the computation. We then optimize the stepwise update rules and give concrete circuit constructions for the resulting controlled arithmetic components. This leads to a modular inversion circuit that uses  $3n + 4\lceil \log_2 n \rceil + O(1)$  logical qubits and  $204n^2 \log_2 n + O(n^2)$  Toffoli gates. By inserting this modular inversion component into the controlled affine point-addition circuit, we obtain a space-efficient algorithm for the ECDLP with  $5n + 4\lceil \log_2 n \rceil + O(1)$  qubits and  $O(n^3)$  Toffoli gates. In particular, for a 256-bit prime-field curve, our estimate reduces the logical-qubit count to 1333, compared with 2124 in the previous low-width implementation of Häner et al.

## 1 Introduction

Elliptic curve cryptography (ECC), first proposed in the mid-1980s as an alternative framework for public-key cryptography [Kob87, Mil85], has become one of the foundational primitives in modern cryptographic systems. The security of ECC-based cryptosystems relies on the computational difficulty of the Elliptic Curve Discrete Logarithm Problem (ECDLP). Specifically, given an elliptic curve defined over a finite field, a base point  $P$  on that curve, and another point  $Q$  resulting from scalar multiplication of  $P$  by an unknown integer  $m$ , the ECDLP asks for the recovery of the scalar  $m$  from the two points. Despite decades of research, no classical algorithm is known that solves the ECDLP in polynomial time of bit

---

<sup>\*</sup>Equal contribution.

<sup>†</sup>Corresponding author. Email: tongyangli@pku.edu.cn

length; the best generic attacks, such as Pollard’s rho method, require  $\Theta(\sqrt{p})$  group operations, where  $p$  denotes the field size of the curve which is exponentially large [GG16].

Compared to classical public-key systems such as RSA [RSA78] and finite-field Diffie-Hellman [DH76], ECC offers equivalent security with substantially smaller key sizes. For example, according to NIST recommendations [BD20], a 256-bit elliptic curve provides a security level of 128 bits, which is comparable to that of RSA with a 3072-bit modulus. This efficiency advantage has led to the widespread adoption of ECC in both theoretical cryptographic constructions and real-world applications. Specifically, ECC is used for key exchange [DH76] and digital signature schemes [EIG85, JMV01] in widely deployed protocols, including transport layer security [BWBG<sup>+</sup>06], secure shell [SG09], and in cryptocurrencies like Bitcoin [BWQ99, NB08].

In contrast to the computational hardness of ECDLP on classical computers, the security landscape changes fundamentally in the presence of large-scale quantum computers. In 1994, **Shor introduced a quantum algorithm that can solve integer factorization and discrete logarithm problems** in polynomial time [Sho94]. Subsequent work showed that Shor’s algorithm can be generalized to elliptic curve groups [PZ03], implying that the ECDLP can also be efficiently solved on a fault-tolerant quantum computer and hence undermines the security of ECC.

At the same time, the practical implementation of quantum algorithms for cryptography problems remains severely constrained by the limitations of near-term quantum hardware. For instance, implementing Shor’s algorithm at cryptographically relevant scales requires a fault-tolerant quantum computer with a large number of logical qubits and circuits, as well as sufficiently low physical error rates (or equivalently achievable logical error rates after error correction) [GE21, Gid25]. Improvements in one dimension often come at the cost of others [RNSL17, HJN<sup>+</sup>20], making realistic resource optimization a delicate trade-off rather than a single-objective problem.

Motivated by these challenges, a substantial body of work has focused on reducing the quantum resource requirements of Shor’s algorithm for integer factorization [Reg25, RV24, KMRV<sup>+</sup>K25, CFS25]. In particular, Chevignard et al. [CFS25] demonstrated that RSA-2048 can be factored using approximately 1730 logical qubits. By comparison, existing resource estimates indicate that solving the ECDLP on ECC-224, which offers a comparable classical security level, still requires at least 1862 logical qubits [RNSL17, HJN<sup>+</sup>20].

On the other hand, early systematic resource estimates for solving the ECDLP were provided by Roetteler et al. [RNSL17] and later refined in [HJN<sup>+</sup>20]. Subsequent studies investigated the impact of curve representations and field choices, with results exploring resource optimization on circuit depth [KJW<sup>+</sup>26], under specific hardware constraints [GYCM25], and several works suggesting that ECDLP over binary elliptic curves may admit more resource-efficient quantum implementations than prime-field curves [BB<sup>+</sup>HL20, PWLK22, JKL<sup>+</sup>22, TT23, JSB<sup>+</sup>25].

These comparisons highlight that, despite extensive prior work, the quantum space requirements for solving the ECDLP remain relatively high, making the reduction of space usage a natural and important objective in the design of quantum ECDLP algorithms.

An important early theoretical result in this direction appeared in 2003, where Proos and Zalka [PZ03] proposed an algorithmic approach via register sharing achieving an attractive asymptotic space bound of

$5n + O(\sqrt{n})$  for solving the ECDLP over an  $n$ -bit prime field. Such a strategy was also recently adopted to qubit cost analysis among quantum algorithms for Decoded Quantum Interferometry (DQI) [KSG<sup>+</sup>25]. However, this result was derived at a high level of abstraction and did not include explicit quantum circuit constructions. As a consequence, several issues critical for practical implementation were left unaddressed, including reversibility, ancilla management, and concrete resource estimation. Moreover, the proposed approach incurs a fidelity loss of  $O(n^{-1})$  arising from the approximate treatment of modular inversion, which further complicates its direct realization within the standard quantum circuit model. As a result, it remains unclear to what extent the stated space bound can be achieved by a fully implementable quantum algorithm, leaving a practically relevant gap that has also been noted in subsequent resource estimation studies such as [RNSL17].

In conclusion, the motivation of our work can be summarized in one sentence:

*Can the quantum space requirements for solving the ECDLP be further reduced in practice?*

## Contributions

Our main contribution is reducing the logical qubit requirements for solving ECDLP within the standard quantum circuit model. Building on the algorithmic framework of Proos and Zalka [PZ03], we present an explicit and fully reversible realization that achieves the previously established low-space bound at the circuit level, while remaining exactly correct, in contrast to the fidelity loss incurred in [PZ03]. Specifically, our contributions are two-fold as follows.

**Space-efficient, reversible algorithm design for modular inversion.** We focus on modular inversion for computing  $|x\rangle|0\rangle \rightarrow |x\rangle|x^{-1} \bmod p\rangle$  with  $x \in \mathbb{F}_p$ , which contributes the dominant component of the logical qubit requirement for solving ECDLP. We develop a fully reversible algorithm for modular inversion based on the Extended Euclidean Algorithm (EEA), with details given in Section 3.1. Table 1 and Table 2 compare the logical qubit requirements for modular inversion in our work with those in previous studies.

Source	Number of logical qubits	Remark
[PZ03] without register sharing	$5n + 4 \log_2 n + O(1)$	without explicit circuit implementation
[PZ03] with register sharing	$3n + 8\sqrt{n} + 4 \log_2 n + O(1)$	
[RNSL17]	$7n + 2 \log_2 n + O(1)$	with explicit circuit implementation
[HJN <sup>+</sup> 20]	$7n + \log_2 n + O(1)$	
<b>This work</b>	$3n + 4 \log_2 n + O(1)$	

Table 1: Comparison of the number of logical qubits required for modular inversion in ECDLP.

A central contribution of our work is a refined and explicit use of the register sharing strategy at the algorithmic level, as described in Section 3.2. In the original construction of [PZ03], the same register resources are allocated to all input values  $x \in \mathbb{F}_p$  in superposition. This uniform allocation results in an  $O(\sqrt{n})$  space overhead and requires truncating outlier values of  $x$ , which in turn introduces an  $O(n^{-2})$  fidelity loss. In contrast, we introduce an exact register allocation strategy that allows deterministic

Source	Number of logical qubits					
	ECC-160	ECC-192	ECC-224	ECC-256	ECC-384	ECC-521
[RNSL17]	1466	1754	2042	2338	3492	4727
[HJN+20]	1350	1606	1862	2124	3151	4258
<b>This work</b>	849	1009	1169	1333	1973	2662

Table 2: Comparison of the concrete number of logical qubits required for Shor’s algorithm.

register usage across different input values  $x \in \mathbb{F}_p$ . This strategy reduces the additional space overhead to  $O(\log n)$  and ensures exact correctness for modular inversion.

Starting from a baseline reversible realization of our space-efficient Extended Euclidean Algorithm, we further introduce a sequence of algorithmic optimizations in Section 3.3, that reorganize the update processes and remove redundant arithmetic operations. To ensure correctness and reversibility, we provide complete algorithm pseudocode (Algorithm 3) together with concrete classical execution examples (Table 4). These examples show that every step of the algorithm is exactly reversible and correct, and can be translated into a quantum circuit.

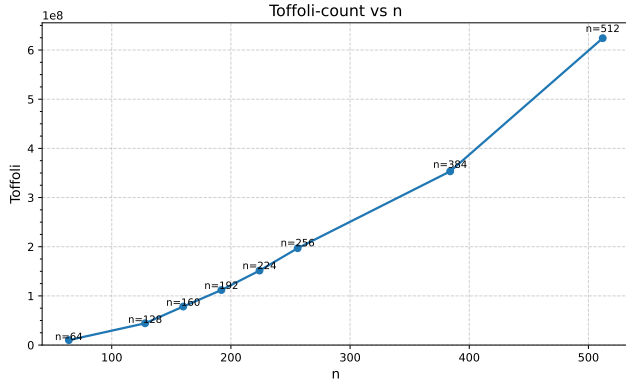
**Explicit quantum circuit construction and resource estimation for modular inversion.** To further show that our space-efficient algorithm for modular inversion is practically realizable, we present a detailed quantum circuit implementation in Section 4. We begin by introducing the overall framework of the circuit implementation (shown in Figure 5 and Figure 6). We then describe the detailed implementations of all building blocks (shown in Figure 7 through Figure 9).

We emphasize that these building blocks are non-standard components whose implementations are highly non-trivial. Consequently, the constructions presented here may not be optimal with respect to gate complexity or circuit depth.

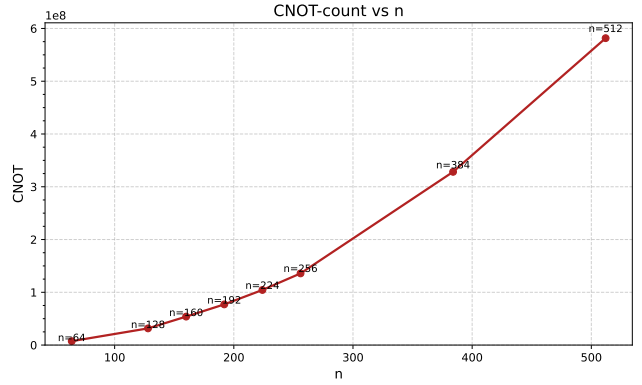
Finally, we provide resource estimates for our quantum circuit implementation. We show in Section 5.2 that one modular inversion requires approximately  $204n^2 \log_2 n + O(n^2)$  Toffoli gates and about  $102n^2 \log_2 n$  CNOT gates asymptotically. In addition, we present numerical evaluations of the Toffoli and CNOT gate counts as functions of the problem size  $n$ , as illustrated in Figure 1. We also merge our modular-inversion component into the full quantum circuit for solving the ECDLP and achieve an algorithm with  $5n + 4\lceil \log_2 n \rceil + O(1)$  qubits and  $976n^3 + O\left(\frac{n^3}{\log_2 n}\right)$  Toffoli gates in total (see Section 5.4).

**Open questions and concurrent work.** Our modular inversion circuit design serves as a general-purpose building block and is not limited to applications in elliptic curve cryptography. We expect that future work may further optimize its quantum gate counts and circuit depth, explore implementations and performance analysis on current quantum architectures, and extend this modular inversion block to other quantum algorithms.

During the preparation of this manuscript, Cheignard, Fouque, and Schrottenloher [CFS26] also proposed a quantum algorithm for ECDLP that reduces the number of qubits. Their improvement comes from the application of a residue number system to compute the projective coordinates of point



(a) Toffoli-Count



(b) CNOT-count

Figure 1: Toffoli gate count and CNOT gate count for modular inversion in ECDLP.

multiplication, whereas our improvement comes from better implementation of the modular inversion by EEA. In terms of total Toffoli count, our algorithm achieves  $O(n^3)$  while their algorithm is  $O(n^4(\log n)^2)$ .

Babbush et al. [BZG<sup>+</sup>26] claimed implementation of Shor’s algorithm for ECDLP with significantly improved total Toffoli count. Because their technical details are not disclosed, we cannot make an explicit comparison with their work. In contrast, we present our implementation details as well as open-sourced repository (see Footnote 2).

## 2 Preliminaries

This section provides a very brief discussion of the basic concepts used in this work. We assume that readers have basic knowledge of quantum computation. For a general survey of quantum computation, we recommend the survey written by Childs and van Dam [CvD10].

### 2.1 Quantum computing and the Toffoli networks

We write basis quantum states as  $|x\rangle$ , where  $x$  is a bit string, and we model a quantum algorithm as a circuit composed of elementary gates applied to one or more qubits. A key feature is that circuits can create and transform superpositions of basis states, enabling interference effects that are exploited by quantum algorithms.

At the fault-tolerant logical level it is common to express circuits over a universal gate set such as Clifford+ $T$  [NC10]. In many architectures the  $T$  gate is substantially more expensive than Clifford operations, so circuit cost is frequently summarized by  $T$ -count,  $T$ -depth, or related metrics [FMMC12]. For design and validation, however, it is often convenient to use a purely reversible gate basis.

Accordingly, we express the main reversible components as *Toffoli networks*. The Toffoli gate maps

$$|x, y, z\rangle \mapsto |x, y, z \oplus (xy)\rangle,$$

and it forms a universal primitive for classical reversible computation [NC10]. A practical benefit of working at the Toffoli-network level is that such networks admit exact realizations over Clifford+T [AMMR13], avoiding approximation overhead associated with synthesizing arbitrary unitaries. Moreover, Toffoli-based reversible circuits can be efficiently simulated on classical inputs at scales far beyond what is possible for general quantum-state simulation, which makes testing and debugging large arithmetic circuits significantly more tractable [HRS17]. For these reasons, we specify the core arithmetic and elliptic-curve routines using Toffoli and CNOT gates.

## 2.2 Elliptic curves and the ECDLP

Let  $p$  be a large prime and let  $\mathbb{F}_p$  denote the finite field with  $p$  elements. An elliptic curve  $E/\mathbb{F}_p$  (in short Weierstrass form) is the set of affine solutions  $(x, y) \in \mathbb{F}_p^2$  to an equation  $y^2 = x^3 + ax + b$ , together with a distinguished point  $\mathcal{O}$  at infinity. The set of  $\mathbb{F}_p$ -rational points, together with  $\mathcal{O}$ , is denoted as  $E(\mathbb{F}_p)$ .

The points on  $E(\mathbb{F}_p)$  form an abelian group under the elliptic-curve addition law, with identity element  $\mathcal{O}$ . For affine points  $P_1 = (x_1, y_1)$  and  $P_2 = (x_2, y_2)$  that are not inverse to each other, the sum  $P_3 = P_1 + P_2$  can be computed via a slope parameter  $\lambda$ :

$$x_3 = \lambda^2 - x_1 - x_2, \quad y_3 = \lambda(x_1 - x_3) - y_1,$$

where  $\lambda$  equals the chord slope  $\frac{y_2 - y_1}{x_2 - x_1}$  when  $P_1 \neq P_2$ , and the tangent slope  $\frac{3x_1^2 + a}{2y_1}$  when  $P_1 = P_2$ . Exceptional cases (e.g.,  $P_i = \mathcal{O}$  or  $P_2 = -P_1$ ) are handled according the standard group properties.

For an integer  $m \geq 1$ , the notation  $[m]P$  denotes the  $m$ -fold sum of a point  $P$  with itself, i.e.  $[m]P = P + P + \dots + P$ , where  $P$  occurs  $m$  time(s). This  $m$ -fold sum can be extended to all  $m \in \mathbb{Z}$  by defining  $[0]P = \mathcal{O}$  and  $[-m]P = [m](-P)$  for  $m \geq 1$ . The operation  $m \mapsto [m]P$  is called *scalar multiplication* and is the core primitive used in elliptic-curve cryptography.

Let  $P \in E(\mathbb{F}_p)$  generates a cyclic subgroup  $\langle P \rangle$  of order  $r$ , and let  $Q \in \langle P \rangle$ . The *elliptic-curve discrete logarithm problem (ECDLP)* is to recover the unique  $m \in \{0, 1, \dots, r - 1\}$  such that

$$Q = [m]P.$$

In classical settings, the best generic algorithms require on the order of  $\Theta(\sqrt{p})$  group operations [GG16], which is exponential in the bit length  $\log_2 p$ .

### 2.2.1 Shor's quantum algorithm for ECDLP

Shor's discrete-logarithm algorithm for solving ECDLP applies to elliptic curve over any finite abelian group and therefore to  $E(\mathbb{F}_p)$ . Let  $n = \lfloor \log_2 p \rfloor + 1$  be the bit-length of  $p$ . The quantum procedure uses two exponent registers and one register storing an elliptic curve point.

Firstly, initialize two  $(n + 1)$ -qubit registers<sup>1</sup> to be  $|0^{n+1}, 0^{n+1}\rangle$ , and apply Hadamard gate to all the qubits to obtain a uniform superposition over pairs  $(k, \ell) \in \{0, 1, \dots, 2^{n+1} - 1\}^2$ . Next, coherently

---

<sup>1</sup>Hasse's bound [Has36] indicates that  $\text{ord}(P) \leq \#E(\mathbb{F}_p) \leq p + 1 + 2\sqrt{p}$ , which can be represented by at most  $n + 1$  bits.

compute the elliptic curve group action into an accumulator as

$$\sum_{k,\ell=0}^{2^{n+1}-1} |k, \ell\rangle |\mathcal{O}\rangle \mapsto \sum_{k,\ell=0}^{2^{n+1}-1} |k, \ell\rangle |[k]P + [\ell]Q\rangle. \quad (1)$$

After this step, apply Quantum Fourier Transform  $\text{QFT}_{2^{n+1}}$  to both exponent registers and then measure them. Finally, a classical post-processing procedure uses the measurement outcomes to reconstruct the discrete logarithm  $m$  with high probability, as shown in [Sho94].

In terms of resource, the dominant cost arises from the coherent group evaluation, i.e., the double-scalar multiplication on elliptic curve points. To reduce the qubit cost associated with QFT, its full circuit on the exponent registers can be replaced by a semiclassical variant [GN96]. This semiclassical Fourier transform performs measurements during the computation, reusing qubits and applying conditional phase rotations based on previously observed outcomes. The overall quantum circuits of Shor's algorithm for ECDLP using QFT (resp. semiclassical QFT) are shown in Figure 2 (resp. Figure 3).

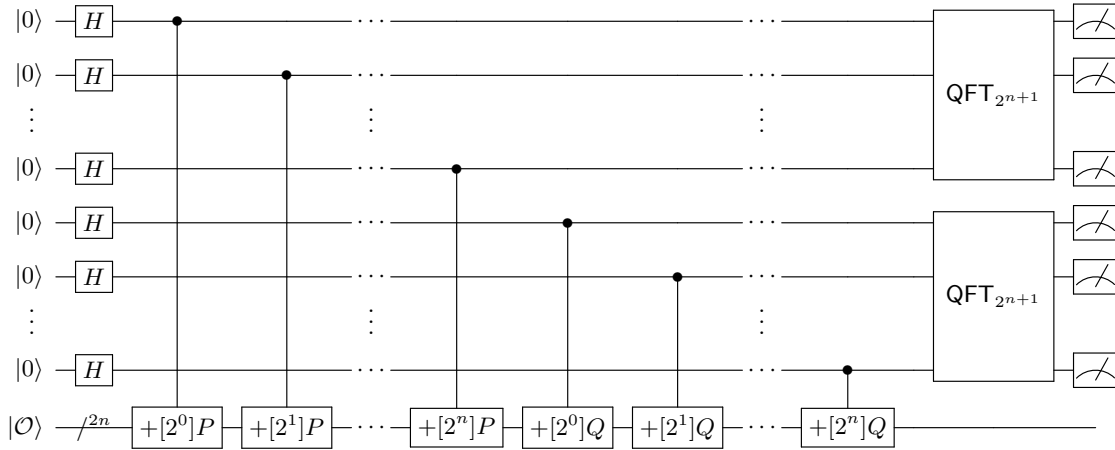


Figure 2: The overall quantum circuit of Shor's algorithm for solving ECDLP using QFT. The qubits, from top to bottom, correspond to the exponent registers containing  $k$  and  $\ell$  in Equation 1 (ordered from lower-order bits to higher-order bits), and to the register that stores the elliptic curve point accumulator.

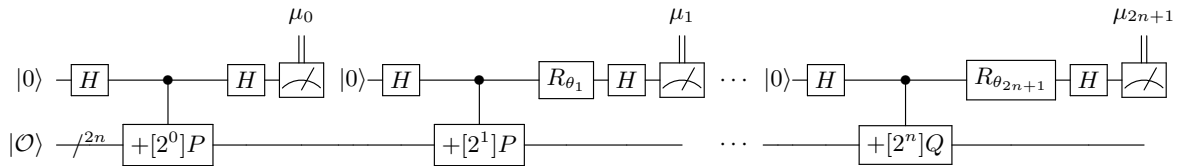


Figure 3: The overall quantum circuit of Shor's algorithm for solving ECDLP using semiclassical QFT. The gates  $R_{\theta_i}$  denote rotation gates with rotation angle  $\theta_i = \sum_{j=0}^{i-1} 2^{i-j} \mu_j$ , where the values  $\mu_j \in \{0, 1\}$  are outcomes obtained in previous measurements. By employing the semiclassical QFT, the exponent register requires only a single qubit, resulting in a reduction of  $2n + 1$  qubits compared to the standard implementation.

### 3 Space-Efficient Extended Euclidean Algorithm

As discussed in previous sections, the dominant cost in designing quantum circuits for solving ECDLP via Shor’s algorithm arises from coherent group additions on elliptic curve points. Among these operations, modular inversion is the most resource-consuming component. In this section, we present a space-efficient and reversible algorithm for modular inversion based on the Extended Euclidean Algorithm. This design is suitable for further translation into a quantum circuit, as detailed in Section 4.

Suppose that  $p > x$  are two positive integers. The well-known *Euclidean algorithm* can be used to compute the greatest common divisor (GCD) of  $p$  and  $x$ . The algorithm initializes  $r_0 := p$  and  $r_1 := x$ , and for iterations  $i = 1, 2, \dots$ , it repeatedly divides  $r_{i-1}$  by  $r_i$  to obtain the quotient  $q_i = \lfloor r_{i-1}/r_i \rfloor$  and the remainder  $r_{i+1} = r_{i-1} - q_i r_i$ . The process terminates when  $r_{k+1} = 0$ , at which point the greatest common divisor of  $p$  and  $x$  equals  $r_k$ .

The *Extended Euclidean Algorithm (EEA)* not only computes the GCD of  $p$  and  $x$ , but also outputs the modular inverse  $x^{-1} \bmod p$  when  $p$  and  $x$  are coprime. In addition to computing the sequence  $r_i$ , it also initializes  $t_0 := 0$  and  $t_1 := 1$ , and for each iteration  $i = 1, 2, \dots$ , updates  $t_{i+1} = t_{i-1} + q_i t_i$  after obtaining  $q_i = \lfloor r_{i-1}/r_i \rfloor$ . When the algorithm first encounters  $r_k = 1$ , the modular inverse is given by  $(-1)^{k-1} t_k \bmod p$ .

When realizing the Extended Euclidean algorithm on a quantum computer to compute the modular inverse of  $x$  with a prime modulus  $p$  of  $n$  binary digits, the primary challenge lies in handling superpositions of  $x$ . The number of iterations required varies from 1 to  $O(n)$  depending on the input, implying that a straightforward implementation would require  $O(n)$  iterations. Each iteration involves divisions and multiplications on  $n$ -digit numbers, leading to an overall gate complexity of  $O(n^3)$ .

In what follows, we describe the dedicated four-phase algorithm framework first proposed in [PZ03], followed by our own algorithmic optimizations and the details of our optimized circuit implementation.

#### 3.1 The four-phase algorithm framework

The four-phase algorithm framework was originally introduced in [PZ03]. It operates on six quantum registers, denoted as  $r_{i-1}$ ,  $r_i$ ,  $t_{i-1}$ ,  $t_i$ ,  $q_i$ , and  $\ell$ , where the first five registers correspond to the variables used in the  $i$ -th iteration of EEA. To compute the quotient  $q_i = \lfloor r_{i-1}/r_i \rfloor$ , the algorithm performs a binary long-division procedure consisting solely of bit shifts and long additions or subtractions. The algorithm proceeds through the following four phases:

- **Phase 1.** The register containing  $r_i$  are repeatedly shifted left by one bit, while the shift counter  $\ell$  is incremented at each step. This continues until the inequality  $2^\ell r_i > r_{i-1}$  holds. Conceptually, this phase determines the largest power of two by which  $r_i$  can be multiplied without exceeding  $r_{i-1}$ . Equivalently, it identifies the bit-length of the binary representation of  $q_i$ , which we denote by  $\ell_0$ .
- **Phase 2.** The register containing  $r_i$  are then shifted right by one bit per step, with  $\ell$  decremented

accordingly. At each step, the registers corresponding to  $r_{i-1}$  and  $q_i$  are updated as

$$(r_{i-1} - q'r_i, q') \rightarrow (r_{i-1} - (q' + 2^\ell q_{i,\ell})r_i, q' + 2^\ell q_{i,\ell}),$$

depending on whether  $r_{i-1} - q'r_i$  remains greater than  $2^\ell r_i$ . Here  $q'$  denotes the current partial quotient, given by  $q' = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \dots + 2^{\ell+1} q_{i,\ell+1}$ , representing the most significant bits accumulated so far in the binary expansion

$$q_i = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \dots + q_{i,0}.$$

This iterative process ultimately yields the transformation

$$(r_{i-1}, 0) \rightarrow (r_{i-1} - q_i r_i, q_i),$$

completing the computation of  $q_i$ .

- **Phase 3.** The register containing  $t_i$  are shifted left by one bit per step, and  $\ell$  is incremented correspondingly. The registers associated with  $t_{i-1}$  and  $q_i$  are updated as

$$(t_{i-1} + q''t_i, q') \rightarrow (t_{i-1} + (q'' + 2^\ell q_{i,\ell})t_i, q'),$$

where the update depends on the bit value  $q_{i,\ell}$  of  $q_i$ . After each step,  $q_{i,\ell}$  is reset to 0, depending on whether  $t_{i-1} + (q'' + 2^\ell q_{i,\ell})t_i > 2^\ell t_i$ . Here  $q'$  and  $q''$  represent the most and least significant portions of the quotient, respectively:

$$q' = 2^{\ell_0} q_{i,\ell_0} + 2^{\ell_0-1} q_{i,\ell_0-1} + \dots + 2^\ell q_{i,\ell}, \quad q'' = 2^{\ell-1} q_{i,\ell-1} + 2^{\ell-2} q_{i,\ell-2} + \dots + q_{i,0}.$$

After completing all steps, the registers corresponding to  $t_{i-1}$  and  $q_i$  are updated as

$$(t_{i-1}, q_i) \rightarrow (t_{i-1} + q_i t_i, 0).$$

- **Phase 4.** Finally, the register containing  $t_i$  are repeatedly shifted right by one bit, and  $\ell$  is decremented at each step. The process terminates once  $\ell = 0$ .

Upon completion of all four phases, a SWAP gate is applied between the register pairs corresponding to  $(r_{i-1}, r_i)$  (which is currently  $(r_{i+1}, r_i)$ ) and the register pairs corresponding to  $(t_{i-1}, t_i)$  (which is currently  $(t_{i+1}, t_i)$ ), respectively. This completes one full iteration of the EEA implementation.

We emphasize that, during the execution of this four-phase algorithm, the correspondence between the iteration index in EEA and the phase number may vary depending on the input value  $x$ . In other words, the algorithm's internal progression through iterations and phases is input-dependent. To avoid ambiguity in the subsequent descriptions, we use “step” to represent any sub-iteration occurring within any phase of an EEA iteration. The example in Table 3 illustrates how the step status evolves for different input values under this four-phase framework.

Although the sequence of step statuses differs for each input  $x$ , the total number of steps required to reach an index  $k$  such that  $r_{k-1} = 1, r_k = 0$  can be bounded within the interval  $[4n, 4\lceil cn \rceil]$  with

Input	$x_1$	$x_2$	$x_3$
Step 1	Iteration 1, Phase 1	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 2	Iteration 1, Phase 1	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 3	Iteration 1, Phase 2	Iteration 1, Phase 1	Iteration 1, Phase 1
Step 4	Iteration 1, Phase 2	Iteration 1, Phase 1	Iteration 1, Phase 2
Step 5	Iteration 1, Phase 3	Iteration 1, Phase 1	Iteration 1, Phase 2
Step 6	Iteration 1, Phase 3	Iteration 1, Phase 2	Iteration 1, Phase 2
Step 7	Iteration 1, Phase 4	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 8	Iteration 1, Phase 4 (and SWAP)	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 9	Iteration 2, Phase 1	Iteration 1, Phase 2	Iteration 1, Phase 3
Step 10	Iteration 2, Phase 1	Iteration 1, Phase 2	Iteration 1, Phase 4
Step 11	Iteration 2, Phase 1	Iteration 1, Phase 3	Iteration 1, Phase 4
Step 12	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 1, Phase 4 (and SWAP)
Step 13	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 2, Phase 1
Step 14	Iteration 2, Phase 2	Iteration 1, Phase 3	Iteration 2, Phase 1
Step 15	Iteration 2, Phase 3	Iteration 1, Phase 3	Iteration 2, Phase 2
Step 16	Iteration 2, Phase 3	Iteration 1, Phase 4	Iteration 2, Phase 2
...	...	...	...
Step 100	Iteration 9, Phase 3	Iteration 5, Phase 2	Iteration 8, Phase 4
...	...	...	...

Table 3: An example illustrating that the iteration index in EEA. The phase number may vary depending on the input value  $x$ .

$c = 1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$ , as formally proven in Appendix A.1. This bounded-step property is crucial for quantum implementation: it implies that a quantum circuit corresponding to one “step” can be repeated at most  $4\lceil cn \rceil \approx 5.76n$  times to definitely obtain the modular inverse of any input  $x$  in superposition. Since each step involves arithmetic operations such as shifts, additions, and subtractions, which require  $O(n)$  quantum gates, the overall gate complexity of the algorithm is reduced to  $O(n^2)$ .

Keeping the above discussion in mind, the complete space-efficient EEA for computing the modular inverse  $x^{-1} \bmod p$ , where  $p$  is a prime represented with  $n$  binary digits and  $x \in \{1, 2, \dots, p-1\}$ , is summarized in Algorithm 1. In this context: (i) the register allocation strategy is described in Section 3.2; (ii) Algorithm 3 provides the optimized stepwise iteration designed to minimize gate complexity and ensure quantum reversibility, as further discussed in Sections 3.2 and 3.3; (iii) the preliminary operation of replacing  $x$  by  $p-x$  when  $x > p/2$  guarantees that the entire procedure remains logically reversible under quantum computation.

### 3.2 Space-efficient algorithm by register sharing

In [PZ03], the authors introduced the concept of *register sharing*. The central idea of register sharing is that, during the execution of the EEA, the sequence  $\{r_i\}$  is monotonically decreasing while the sequence  $\{t_i\}$  is monotonically increasing. This complementary behavior allows both values to occupy the same quantum register at different stages of computation, thereby reducing the overall space requirement. The identity

$$r_{i-1}t_i + r_it_{i-1} = p$$

---

**Algorithm 1** Full description of our space-efficient EEA

---

**Require:** Quantum registers  $|x\rangle|0^n\rangle|0^m\rangle$ , where the first  $2n$  qubits hold the input/output data and the remaining  $m$  serve as auxiliary qubits.

**Ensure:** Output state  $|x\rangle|x^{-1} \bmod p\rangle|0^m\rangle$ .

Initialize register **Work1** with  $(n + 3)$  qubits as  $|100, p\rangle$  ▷ Using  $(n + 3)$  auxiliary qubits

Initialize register **Work2** with  $(n + 3)$  qubits as  $|000, x\rangle$  ▷ Pad  $x$  to  $n$  bits on the left

Initialize **Length** registers to  $|\ell_t := 1, \ell_q := 0, \ell_{r'} := \text{length of } x, \ell_s := 0\rangle$

Initialize **Control** registers to  $|\text{Phase1} := 0, \text{Phase2} := 0, \text{Sign} := 0, \text{Iter} := 0\rangle$

**if**  $x > p/2$  **then** ▷ Ensures that the algorithm is invertible

**Iter**  $\leftarrow$  **Iter**  $\oplus$  1

**end if**

**if** **Iter** = 1 **then**

$x \leftarrow p - x$

**end if**

**for**  $i = 1, 2, \dots, 4\lceil cn \rceil$  **do** ▷ Main iterative loop performing the optimized algorithm steps

Execute Algorithm 3 on the quantum registers

**end for**

Copy the content of  $t'$  in **Work2** to the output register

**if** **Iter** = 0 **then** ▷ The resulting value equals  $(-1)^k t_k$ , where  $k$  is the number of EEA iterations

**Output**  $\leftarrow p - \text{Output}$

**end if**

**for**  $i = 1, 2, \dots, 4\lceil cn \rceil$  **do** ▷ Reverse computation to recompute  $x$

Execute the inverse of Algorithm 3 on the quantum registers

**end for**

**if** **Iter** = 1 **then** ▷ Undo the earlier transformation  $x \leftarrow p - x$

$x \leftarrow p - x$

**end if**

**if**  $x > p/2$  **then**

**Iter**  $\leftarrow$  **Iter**  $\oplus$  1

**end if**

Reset all auxiliary qubits to  $|0\rangle$ .

---

implies that two quantum registers, each consisting of  $(n + 2)$  qubits, are sufficient: one to store the pair  $(r_{i-1}, t_i)$  and the other to store  $(r_i, t_{i-1})$ .

We extend this register-sharing idea further. Specifically, we observe that a single quantum register of  $(n + 2)$  qubits can be used to store the triple  $(r_{i-1}, t_i, q_i)$  simultaneously, including the intermediate states that arise during phases 2 and 3 of the algorithm. These phases are responsible for computing  $q_i = \lfloor r_{i-1}/r_i \rfloor$  and updating the variables

$$r_{i-1} \leftarrow r_{i-1} - q_i r_i, t_{i-1} \leftarrow t_{i-1} + q_i t_i.$$

The detailed allocation of quantum registers is described as follows, and illustrated in Figure 4.

- **Work1 register (of  $(n + 3)$  qubits).** The left-most  $\ell_t + 1$  qubits encode the value  $t := t_i$  in little-endian order (here we append a zero to the rightmost position of  $t$  in order to simplify the circuit implementation). The following  $\ell_q$  qubits store the intermediate quotient value  $q := q'$  (only the effective most significant bits) in phases 2 and 3, in big-endian order. The remaining qubits hold the value  $r := r_{i-1}$  (or its updated form  $r := r_{i-1} - q' r_i$ ) in big-endian order.
- **Work2 register (of  $(n + 3)$  qubits).** The right-most  $\ell_{r'}$  qubits store  $r' := r_i$  in big-endian order, while the remaining qubits store the value  $t' := t_{i-1}$  (and its intermediate update  $t' := t_{i-1} + q'' t_i$ ) in little-endian order. During phases 2 and 3, this register may be circularly shifted left by  $\ell_s$  positions. In such cases, the value  $t'$  may span both ends of the register, effectively splitting into two contiguous parts.
- **Length registers.** Four auxiliary registers are used to manage variable-length storage. Three of them each contain  $\lfloor \log_2 n \rfloor + 2$  qubits and store the length indicators  $\ell_t, \ell_q$ , and  $\ell_{r'}$ , respectively. The fourth register, of  $\lfloor \log_2 n \rfloor + 3$  qubits, stores the shift counter  $\ell_s$ . These **Length** registers mark the logical boundaries within the **Work1** and **Work2** registers and enable coherent manipulation of superposed inputs of varying lengths.
- **Control registers.** Two single-qubit **Phase** registers indicate the current phase of the four-phase algorithmic framework, and one single-qubit **Iter** register that records the parity of the current EEA iteration number. Additionally, there are two auxiliary single-qubit registers, **Sign** and **Ctrl**, used for intermediate flag and control operations.

We next describe the behavior of the system when performing comparison, addition, and subtraction operations on the register pairs  $(r, r')$  and  $(t, t')$ . The arithmetic between  $r$  and  $r'$  is relatively straightforward: a left shift by  $\ell_s$  positions corresponds to multiplying  $r'$  by  $2^{\ell_s}$ . In contrast, the arithmetic involving  $t$  and  $t'$  requires a more careful interpretation. A convenient way to view this operation is that a left shift of  $\ell_s$  positions can be regarded as dividing  $t'$  by  $2^{\ell_s}$ , where the integer part is placed in the left-most portion of **Work2**, and the fractional part occupies the right-most portion. When  $t$  is added to the integer part of  $t'$  (which are properly aligned), the arithmetic relation can be expressed as  $2^{-\ell_s} t' + t = 2^{-\ell_s} (t' + 2^{\ell_s} t)$ . Thus, the expression  $t' + 2^{\ell_s} t$  represents the desired result, corresponding to a left shift by  $\ell_s$  positions.

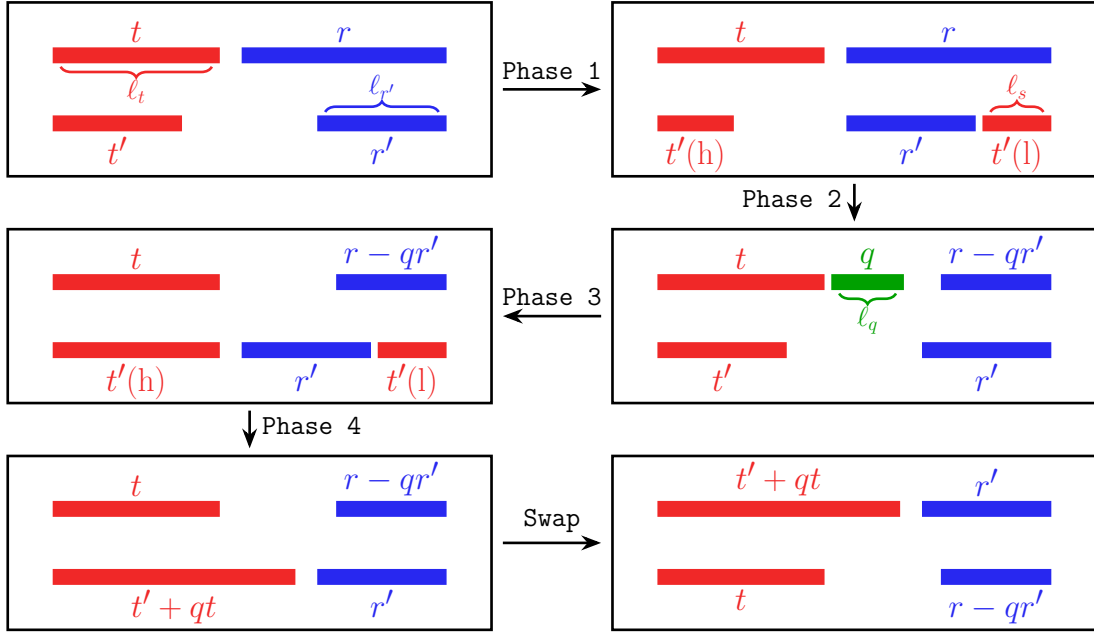


Figure 4: An illustration of how the two `Work` registers are allocated for temporary variables within a single iteration of the EEA. The upper and lower stripes represent the `Work1` and `Work2` registers, respectively. The symbols (h) and (l) indicate that the value  $t'$  is split into its higher-order bits (h) and lower-order bits (l), which are placed at the corresponding positions on the two sides of the `Work2` register.

With this register allocation, one step of our space-efficient EEA proceeds as in Algorithm 2. To illustrate how the proposed space-efficient EEA operates in practice, we also provide a concrete execution example for  $p = 37$  and  $x = 13$ , shown in Table 4.

For each step, Table 4 shows how the contents of the two `Work` registers evolve and how different variables are mapped onto `Work1` and `Work2` under the register-sharing strategy. In particular, the variable  $t'$  stored in `Work2` is divided into two parts that occupy the left-most and right-most portions of the register. The division symbols are not explicitly implemented in the quantum circuit; they are all illustrative and inferred from the corresponding `Length` registers, used to visualize the register allocation. In the actual quantum implementation, all registers are in superposition, and the location of these division symbols may vary across different input values.

### 3.3 Algorithmic optimizations

The baseline implementation of one step, as described in the previous subsection, was constructed to be fully reversible, ensuring that every state transformation can be realized as a unitary operation on a quantum computer. However, this direct implementation contains multiple redundant operations that unnecessarily increase both the circuit depth and gate count. In this subsection, we present a series of algorithmic optimizations applied to the baseline design in order to reduce the quantum circuit depth and overall gate complexity.

---

**Algorithm 2** One step of our EEA implementation with register sharing

---

**Require:** Work1 register stores  $|t, q, r\rangle$ , Work2 register stores  $|t', r'\rangle$

**Require:** Length registers store  $|\ell_t, \ell_q, \ell_{r'}, \ell_s\rangle$

**Require:** Control registers store  $|\text{Phase1}, \text{Phase2}, \text{Iter}, \text{Sign}\rangle$ .

```
if (Phase1, Phase2) = (0, 0) then                                     ▷ Arithmetic logic for the four phases
    Perform a one-position left shift on Work2
     $\ell_s \leftarrow \ell_s + 1$ 
     $\text{Sign} \leftarrow \text{Sign} \oplus (r < 2^{\ell_s r'})$                                ▷ Act on qubits  $(\ell_t + \ell_q + 2)$  through  $(n + 3 - \ell_s)$ 
else if (Phase1, Phase2) = (0, 1) then
    Perform a one-position right shift on Work2
     $\ell_s \leftarrow \ell_s - 1, \ell_q \leftarrow \ell_q + 1$ 
     $(\text{Sign}, r) \leftarrow (\text{Sign}, r) - 2^{\ell_s r'}$                                ▷ Use register Sign to store the sign of the subtraction result
    if Sign = 1 then
         $r \leftarrow r + 2^{\ell_s r'}$                                              ▷ Ignore overflows
    end if
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
    Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1                 ▷ The least significant work qubit of  $q$ 
else if (Phase1, Phase2) = (1, 0) then
    Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1
    if Sign = 0 then
         $t' \leftarrow t' - 2^{\ell_s t}$                                            ▷ Act on left-most  $(\ell_t + 1)$  qubits
    end if
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
     $(\text{Sign}, t') \leftarrow (\text{Sign}, t') + 2^{\ell_s t}$                                ▷ Use register Sign to store the sign of the addition result
    Perform a one-position left shift on Work2
     $\ell_s \leftarrow \ell_s + 1, \ell_q \leftarrow \ell_q - 1$ 
else if (Phase1, Phase2) = (1, 1) then
     $\text{Sign} \leftarrow \text{Sign} \oplus (t' \geq 2^{\ell_s t})$                                ▷ Same qubit range as above
    Perform a one-position right shift on Work2
     $\ell_s \leftarrow \ell_s - 1$ 
end if
if  $\ell_q = 0$  and  $\ell_{r'} > 0$  then                                           ▷ Phase update logic;  $\ell_{r'} = 0$  indicates algorithm termination
     $\text{Phase2} \leftarrow \text{Phase2} \oplus \text{Sign} \oplus \text{Phase1}, \text{Sign} \leftarrow \text{Sign} \oplus \text{Phase2}$ 
end if
if  $\ell_s = 0$  then
     $\text{Phase1} \leftarrow \text{Phase1} \oplus 1, \text{Phase2} \leftarrow \text{Phase2} \oplus 1$ 
end if
if  $\ell_q = 0$  and  $\ell_s = 0$  then                                           ▷ Register swapping at the end of one EEA iteration
    Swap Work1 and Work2
    Update  $\ell_t$  to the bit length of the new  $t$                                ▷ Act on the left-most  $(n + 3 - \ell_{r'})$  qubits of Work1 and Work2
    Update  $\ell_{r'}$  to the bit length of the new  $r'$                              ▷ Act on the right-most  $(n + 2 - \ell_t)$  qubits of Work1 and Work2
     $\text{Iter} \leftarrow \text{Iter} \oplus 1$ 
end if
```

---

Step	Work1	Work2	$t$	$q$	$r$	$t'$	$r'$	$l_t$	$l_q$	$l_{r'}$	$l_s$	Phase1	Phase2	Iter	Sign
0	10 0100101	00000 1101	1	0	37	0	13	1	0	4	0	0	0	0	0
1	10 0100101	0000 1101 0	1	0	37	0	13	1	0	4	1	0	0	0	0
2	10 0100101	000 1101 00	1	0	37	0	13	1	0	4	2	0	1	0	0
3	10 1001011	0000 1101 0	1	2	11	0	13	1	1	4	1	0	1	0	0
4	10 10 01011	00000 1101	1	2	11	0	13	1	2	4	0	1	0	0	0
5	10 1001011	0000 1101 0	1	2	11	0	13	1	1	4	1	1	0	0	0
6	10 0001011	000 1101 01	1	0	11	2	13	1	0	4	2	1	1	0	1
7	10 0001011	1000 1101 0	1	0	11	2	13	1	0	4	1	1	1	0	0
8	010 001101	10000 1011	2	0	13	1	11	2	0	4	0	0	0	1	0
9	010 001101	0000 1011 1	2	0	13	1	11	2	0	4	1	0	1	1	0
10	010 1 00010	10000 1011	2	1	2	1	11	2	1	4	0	1	0	1	0
11	010 000010	1000 1011 1	2	0	2	3	11	2	0	4	1	1	1	1	1
12	110 001011	0100000 10	3	0	11	2	2	2	0	2	0	0	0	0	0
13	110 001011	100000 10 0	3	0	11	2	2	2	0	2	1	0	0	0	0
14	110 001011	00000 10 01	3	0	11	2	2	2	0	2	2	0	0	0	0
15	110 001011	0000 10 010	3	0	11	2	2	2	0	2	3	0	1	0	0
16	110 1 00011	00000 10 01	3	4	3	2	2	2	1	2	2	0	1	0	0
17	110 10 0011	100000 10 0	3	4	3	2	2	2	2	2	1	0	1	0	0
18	110 101 001	0100000 10	3	5	1	2	2	2	3	2	0	1	0	0	0
19	110 10 0001	010000 10 1	3	4	1	5	2	2	2	2	1	1	0	0	0
20	110 1 00001	10000 10 10	3	4	1	5	2	2	1	2	2	1	0	0	0
21	110 000001	0100 10 100	3	0	1	17	2	2	0	2	3	1	1	0	1
22	110 000001	00100 10 10	3	0	1	17	2	2	0	2	2	1	1	0	0
23	110 000001	000100 10 1	3	0	1	17	2	2	0	2	1	1	1	0	0
24	100010 010	11000000 1	17	0	2	3	1	5	0	1	0	0	0	1	0
25	100010 010	1000000 1 1	17	0	2	3	1	5	0	1	1	0	0	1	0
26	100010 010	000000 1 11	17	0	2	3	1	5	0	1	2	0	1	1	0
27	100010 1 00	1000000 1 1	17	2	0	3	1	5	1	1	1	0	1	1	0
28	100010 10 0	11000000 1	17	2	0	3	1	5	2	1	0	1	0	1	0
29	100010 1 00	1000000 1 1	17	2	0	3	1	5	1	1	1	1	0	1	0
30	100010 000	100100 1 10	17	0	0	37	1	5	0	1	2	1	1	1	1
31	100010 000	0100100 1 1	17	0	0	37	1	5	0	1	1	1	1	1	0
32	Terminated	Terminated	37	0	1	17	0	6	0	0	0	0	0	0	0
33	Terminated	Terminated	37	0	1	17	0	6	0	0	1	0	0	0	0
34	Terminated	Terminated	37	0	1	17	0	6	0	0	2	0	0	0	0
35	Terminated	Terminated	37	0	1	17	0	6	0	0	3	0	0	0	0
36	Terminated	Terminated	37	0	1	17	0	6	0	0	4	0	0	0	0

Table 4: An execution example of our space-efficient EEA for  $p = 37$  and  $x = 13$ . The table mainly illustrates how the two  $(n + 3)$ -qubit registers **Work1** and **Work2** are allocated during the execution to store the variables  $t, q, r$  and  $t', r'$ , respectively.

**Removing redundant arithmetic and shift operations.** In the baseline version, several arithmetic and shift operations between different phases are functionally redundant. Specifically, we have:

- In phases 1 and 2: comparison, addition, subtraction between  $(r, 2^{\ell_s} r')$ ;
- In phases 3 and 4: comparison, addition, subtraction between  $(t', 2^{\ell_s} t)$ ;
- In phases 1 and 3: a one-position left shift on `Work2`;
- In phases 2 and 4: a one-position right shift on `Work2`.

By combining the control conditions of these operations (or equivalently, the corresponding quantum control wires), we can eliminate redundant operations from the circuit. This optimization results in a total of two location-controlled addition and subtraction, and two location-controlled swaps in one step. Here, *location-control* refers to arithmetic operations applied conditionally on specific positions of the two `Work` registers, with the active positions indicated by the `Length` registers.

**Merging location-controlled swaps.** To further decrease the circuit depth and gate count, we observe that a single location-controlled swap requires  $O(n \log_2 n)$  quantum gates. When two such swaps are merged into a single operation, two additional position shifts on `Work2` are inevitably introduced. Fortunately, this trade-off is beneficial: each position shift requires only  $O(n)$  gates, making the merging optimization asymptotically advantageous.

**Algorithm pseudocode and overall complexity.** After applying the above optimizations, the overall asymptotic quantum resource estimation per step is summarized as follows:

- Five location-controlled arithmetic operations, including one swap, two additions, and two subtraction; along with four length updates at the termination step of an EEA iteration. Each of these operations costs  $O(n \log_2 n)$  gates in a straightforward implementation.
- Four position shifts and one  $(n + 3)$ -qubit SWAP, each requiring  $O(n)$  quantum gates.

With these optimizations, one step of our space-efficient EEA proceeds as in Algorithm 3.

## 4 Quantum Circuit Implementation of Modular Inversion

In this section, we present the explicit quantum circuit implementation of a single step of the space-efficient EEA with register sharing, as described in Algorithm 3. Throughout the section, we use the same quantum register notation as in the algorithm.

The full circuit construction is, however, too complex to be depicted within a small number of circuit diagrams. This difficulty is mainly due to the presence of location-controlled arithmetic operations, which are highly non-standard. To present the construction in a relatively more explicit manner, we first describe the overall circuit structure in Section 4.1, where the location-controlled arithmetic operations are treated as circuit blocks; we then provide a detailed implementation of these operations in Section 4.2. In all circuit diagrams, the black triangle denotes the output wire that carries the result of the corresponding circuit block; and we denote  $\ell = \lfloor \log_2 n \rfloor$  for convenience.

---

**Algorithm 3** Optimized one step of our EEA implementation

---

**Require:** Work1 register stores  $|t, q, r\rangle$ , Work2 register stores  $|t', r'\rangle$ ;

**Require:** Length registers store  $|\ell_t, \ell_q, \ell_{r'}, \ell_s\rangle$ ;

**Require:** Control registers store  $|\text{Phase1}, \text{Phase2}, \text{Iter}, \text{Sign}\rangle$ .

```
if Phase1 = 0 then ▷ Pre-shift operations
  Perform a one-position left shift on Work2, and update  $\ell_s \leftarrow \ell_s + 1$ 
  if Phase2 = 1 then
    Perform a two-position right shift on Work2, and update  $\ell_s \leftarrow \ell_s - 2$ 
  end if
   $(\text{Sign}, r) \leftarrow (\text{Sign}, r) - 2^{\ell_s} r'$  ▷ Arithmetic block 1: location-controlled subtraction on  $r$ 's
  if Phase2 = 1 then
     $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
  end if
  if Phase2 = 0 or Sign = 0 then
     $r \leftarrow r + 2^{\ell_s} r'$ 
  end if
end if
if Phase1  $\oplus$  Phase2 = 1 then ▷ Arithmetic block 2: location-controlled swap
  Swap Sign with the  $(\ell_t + \ell_q + 1)$ -th qubit of Work1
  if Phase1 = 1 then
     $\ell_q \leftarrow \ell_q - 1$ 
  else
     $\ell_q \leftarrow \ell_q + 1$ 
  end if
end if
if Phase1 = 1 then ▷ Arithmetic block 3: location-controlled addition on  $t$ 's
  if Phase2 = 1 or Sign = 0 then
     $t' \leftarrow t' - 2^{\ell_s} t$ 
  end if
   $\text{Sign} \leftarrow \text{Sign} \oplus 1$ 
   $(\text{Sign}, t') \leftarrow (\text{Sign}, t') + 2^{\ell_s} t$ 
  Perform a one-position left shift on Work2, and update  $\ell_s \leftarrow \ell_s + 1$  ▷ Post-shift operations
  if Phase2 = 1 then
    Perform a two-position right shift on Work2, and update  $\ell_s \leftarrow \ell_s - 2$ 
  end if
end if
if  $\ell_q = 0$  and  $\ell_{r'} > 0$  then ▷ Phase update logic;  $\ell_{r'} = 0$  indicates algorithm termination
   $\text{Phase2} \leftarrow \text{Phase2} \oplus \text{Sign} \oplus \text{Phase1}$ ,  $\text{Sign} \leftarrow \text{Sign} \oplus \text{Phase2}$ 
end if
if  $\ell_s = 0$  then
   $\text{Phase1} \leftarrow \text{Phase1} \oplus 1$ ,  $\text{Phase2} \leftarrow \text{Phase2} \oplus 1$ 
end if
if  $\ell_q = 0$  and  $\ell_s = 0$  then ▷ Register swapping at the end of one EEA iteration
  Swap Work1 and Work2
  Update  $\ell_t$  to the bit length of the new  $t$ ,  $\ell_{r'}$  to the bit length of the new  $r'$ 
   $\text{Iter} \leftarrow \text{Iter} \oplus 1$ 
end if
```

---

## 4.1 Overall circuit implementation of one step

According to Algorithm 3, the overall circuit implementation of a single iteration of our space-efficient EEA is shown in Figures 5 and 6, presented in a continuous layout. Both circuit diagrams are divided into several algorithmic components, indicated by dashed boxes. Each component corresponds exactly to one arithmetic block specified in Algorithm 3.

In both circuit diagrams, **Shift** denotes a position shift of the workspace: a positive value represents a left shift, while a negative value represents a right shift. The circuit blocks **Add**, **Sub**, and **Swap** denote location-controlled addition, subtraction, and swap operations, respectively. At the end of each EEA iteration, the circuit block labeled **SWAP** represents a full SWAP operation applied to all qubits in the registers **Work1** and **Work2**; this block is distinct from the **Swap** block to avoid ambiguity. Finally, the **Len** block denotes the update operations on the length registers.

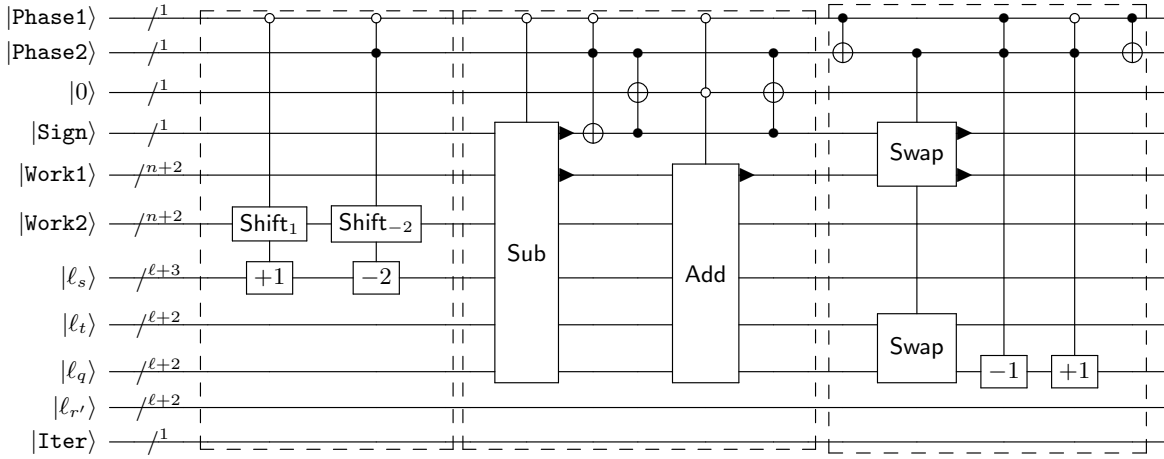


Figure 5: Overall circuit implementation (Part 1) of a single iteration of our space-efficient EEA. The three dashed boxes, from left to right, represent: (1) pre-shift operations; (2) location-controlled subtraction on  $r$ 's; (3) location-controlled swap.

## 4.2 Location-controlled operations

In this subsection, the two **Work** registers are indexed, from left to right, by  $u_1, u_2, \dots, u_{n+3}$  and  $v_1, v_2, \dots, v_{n+3}$ , respectively. In practice, we recommend storing the truth value minus one in all **Length** registers. The reason is that Algorithm 3 contains controlled operations that are performed when the value stored in the **Length** register equals zero. By encoding the value as the truth value minus one, we can detect whether the original truth value equals zero by looking at the sign bit of the **Length** register, avoiding the need to implement a multi-qubit controlled operation over  $\log_2 n$  qubits.

**Location-controlled Add, Sub, Swap circuits.** We first present explicit quantum circuit implementations of the location-controlled arithmetic operations appearing in Figures 5 and 6. The main technical difficulty lies in realizing arithmetic operations whose execution is *coherently controlled* by a location value stored in a different quantum register: unlike standard controlled gates, where the control qubits

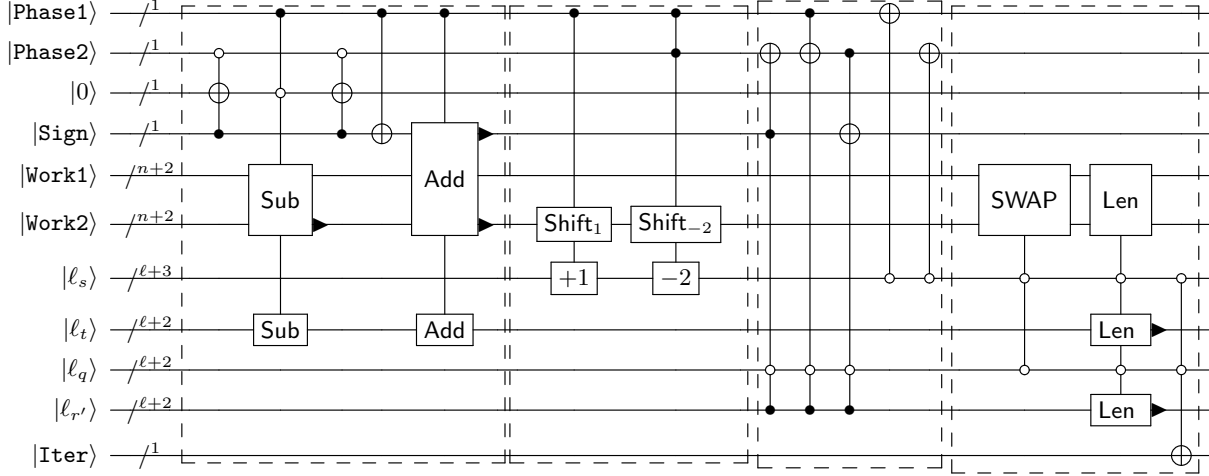


Figure 6: Overall circuit implementation (Part 2) of a single iteration of our space-efficient EEA. The four dashed boxes, from left to right, represent: (1) location-controlled addition on  $t$ 's; (2) post-shift operations; (3) phase update; (4) swapping  $\text{Work1}$  and  $\text{Work2}$ , together with the corresponding length updates at the end of one EEA iteration.

and active qubits are both fixed and local, here the control information specifies *which positions* in the working registers should be acted upon. As a first step toward addressing this challenge, we begin by describing the location-controlled swap circuit, as shown in Figure 7.

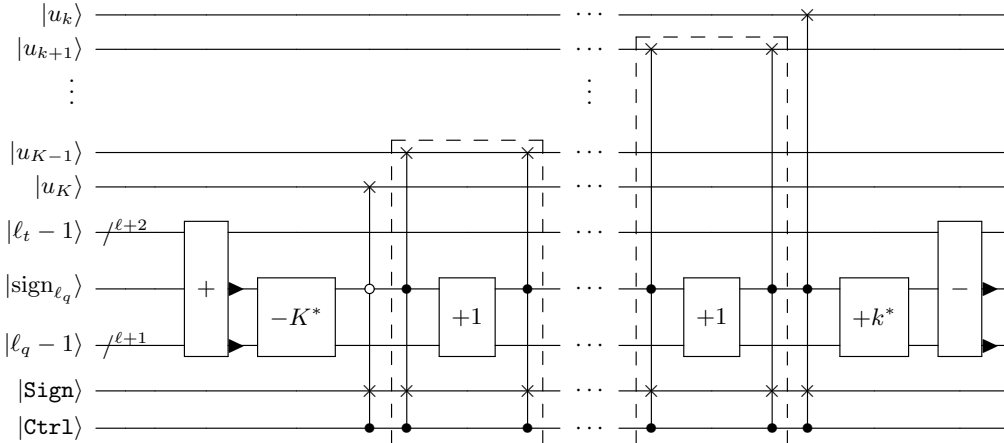


Figure 7: The explicit implementation of a location-controlled swap circuit. This circuit swaps the qubit  $u_{\ell_t + \ell_q + 1}$  from the working space  $\text{Work1}$  and the qubit  $\text{Sign}$ . Here  $K^* = K - 3$ ,  $k^* = k - 2$ . We assume that  $k \leq \ell_t + \ell_q + 1 \leq K$ , where the parameters  $k \leq K$  are known in advance.

To understand the correctness of the location-controlled swap circuit, we observe that a SWAP gate between a qubit at a specific location in  $\text{Work1}$  and the  $\text{Sign}$  qubit is executed, if and only if the two corresponding controlled-SWAP gates around the  $+1$  gate (the dashed boxes in Figure 7) do not cancel each other. More precisely, when  $\ell_t + \ell_q + 1 = j \in [k + 1, K - 1]$ , the two controlled-SWAP gates associated with  $u_j$  differ only in the neighborhood of the  $(K - j)$ -th  $+1$  gate acting on the  $\ell_q$  register. In this case,

these two controlled-SWAP gates are conditioned on different values of  $\text{sign}_{\ell_q}$  and therefore do not cancel each other.

We emphasize that the arithmetic gates acting on the **Length** registers (including the  $+$ ,  $-$ ,  $-K^*$ ,  $+k^*$ , and  $+1$  gates) are not controlled by the **Ctrl** wire, which represents the external control of the entire circuit block. The reason is that these arithmetic operations on the **Length** registers are eventually canceled out, regardless of whether the whole circuit block is activated by external control conditions.

Keeping the implementation principle of the location-controlled swap gate in mind, we next present explicit circuit diagrams for the location-controlled addition/subtraction circuit blocks, adopting the ripple-carry adder using MAJ and UMA blocks [CDKM04], as shown in Figure 8.

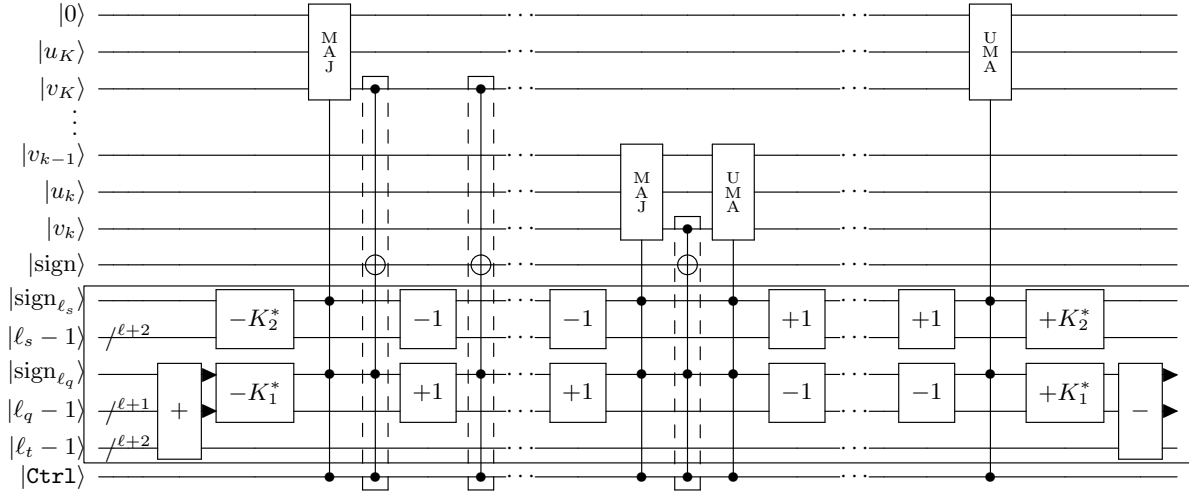


Figure 8: A template for the explicit implementation of a location-controlled addition/subtraction circuit. The circuit in the figure is designed to perform the arithmetic operation  $(\text{Sign}, r) \leftarrow (\text{Sign}, r) - 2^{\ell_s} r'$ . It operates on the qubits indexed from  $(\ell_t + \ell_q + 2)$  to  $(n + 3 - \ell_s)$  on the working registers **Work1** and **Work2**. Here  $K_1^* = K - 3$  and  $K_2^* = n + 3 - K$ . We assume that  $k \leq \ell_t + \ell_q + 2$  and  $n + 3 - \ell_s \leq K$ , where the parameters  $k \leq K$  are known in advance. For the location-controlled addition circuit implementing  $r \leftarrow r + 2^{\ell_s} r'$  without activating the **Sign** register, the Toffoli gates in the dashed boxes can be removed. For the location-controlled addition/subtraction circuits acting on  $t$ 's, the control is one-sided. Therefore, half of the  $\pm K^*$ ,  $\pm 1$  gates inside the solid box, which are used to implement the location-control mechanism, can be omitted.

**Length-update circuits.** Finally, we describe the length-update circuits used at the end of each EEA iteration to update the values of  $\ell_t$  and  $\ell_{r'}$ . We focus on the circuit that updates  $\ell_t$  to the length of the new value of  $t$ , as shown in Figure 9; the circuit for updating  $\ell_{r'}$  is similar and therefore omitted.

To see why this circuit correctly updates the length of  $t$ , it is helpful to first consider a simplified version in which the control on  $\ell_{r'}$  is removed. Inside the dashed box in Figure 9, once the circuit encounters a position  $j$  such that  $u_j = 1$ , the first auxiliary qubit is irreversibly set to 1, which in turn causes the  $+1$  gate to be applied from that point onward. Similarly, once a position with  $v_j = 1$  is encountered, the  $+1$  gate is again permanently activated.

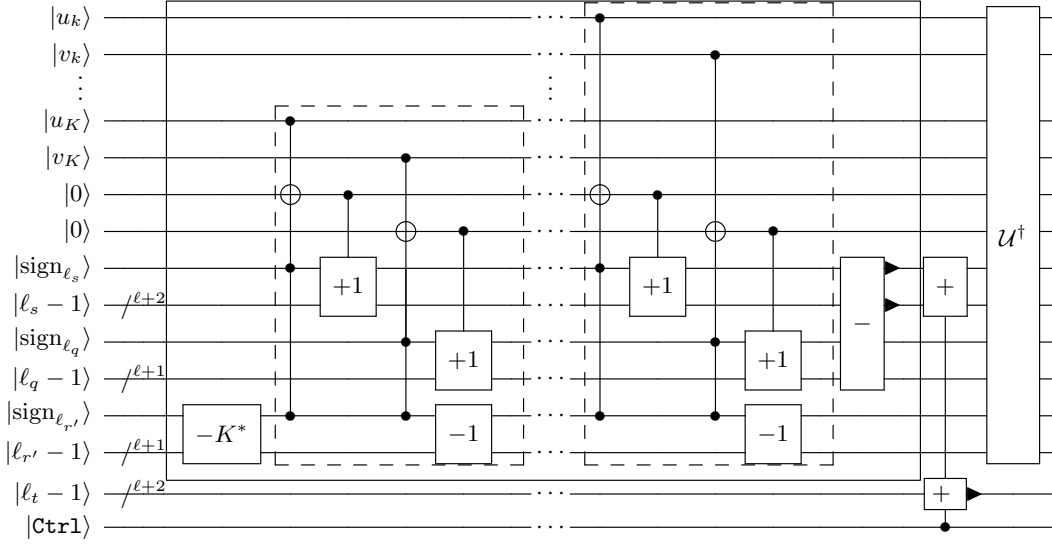


Figure 9: The explicit implementation of the length updating circuit. This circuit updates  $\ell_t$  to the bit length of the new  $t$ . Here,  $K^* = n + 3 - K$ , and  $\mathcal{U}$  denotes the collection of quantum operations in the outer solid box. The bit-wise operations shown in the dashed boxes are applied independently to each qubit pair  $|u_i, v_i\rangle, i = K, K - 1, \dots, k$ . We assume that the previous value of  $\ell_t$  does not exceed  $k$ , and that  $\ell_{r'} \geq n + 3 - K$ , i.e., the updated value of  $\ell_t$  is guaranteed to be at most  $K$ , where the parameters  $k \leq K$  are fixed and known in advance.

As a result, after the loop within the dashed box is completed, the values stored in the registers  $\ell_s$  and  $\ell_q$  differ by exactly the amount equal to the difference between the new and the original lengths of  $t$ . This difference is then added to the register  $\ell_t$ , yielding the correct updated length. Finally, the operation  $\mathcal{U}^\dagger$  uncomputes all auxiliary computations in the outer solid box, restoring the auxiliary registers to their original states.

### 4.3 Step-dependent active windows

To reduce the quantum gate complexity for implementing our space-efficient EEA, we introduce step-dependent active windows for each location-controlled operation. As illustrated in the figures of the previous subsection, we define  $k$  and  $K$  as known bounds on the active indices of the `Work` registers.

For instance, at step  $T$ , a location-controlled Swap circuit acts on the  $(\ell_t + \ell_q + 1)$ -th qubit of the `Work1` register. Over all possible inputs  $x$  used to compute the modular inverse  $x^{-1} \bmod q$ , the quantity  $\ell_t + \ell_q + 1$  is bounded below by  $k := k(T)$  and above by  $K := K(T)$ . Therefore, applying location-controlled operations to qubits in the `Work1` register with indices outside the interval  $[k, K]$  is unnecessary. We refer to this interval as the *active window*.

We next specify the step-dependent active windows for each type of location-controlled operation. All bounds are taken over all *possible inputs*  $x$ , namely, those inputs  $x$  for which the location-controlled circuits are activated by the outer control qubits. The constant  $c$  equals to  $1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$ . We defer the proofs to Appendix A.2.

- **Location-controlled addition/subtraction on  $r$ 's.** These operations act on qubits indexed from  $(\ell_t + \ell_q + 2)$  to  $(n + 3 - \ell_s)$ . The upper bound  $K_1 = K_1(T) = n + 3$ ; the lower bound  $k_1 = k_1(T)$  is defined by

$$\ell_t + \ell_q + 2 \geq k_1(T) := \max \left\{ \left\lceil \frac{T - n - 2}{4c - 1} \right\rceil, 1 \right\} + 2.$$

- **Location-controlled swap.** These operations act on the  $(\ell_t + \ell_q + 1)$ -th qubit. The two-sided bounds are defined by

$$\begin{aligned} \ell_t + \ell_q + 1 &\geq k_2(T) := \max \left\{ \left\lceil \frac{T - 3(n + 2)}{4c - 3} \right\rceil, 1 \right\} + 1, \\ \ell_t + \ell_q + 1 &\leq K_2(T) := \min \{ \lfloor T/2 \rfloor + 2, n + 2 \}. \end{aligned}$$

- **Location-controlled addition/subtraction on  $t$ 's.** These operations act on the first  $(\ell_t + 1)$  qubits. This is a one-sided controlled operation, the upper bound  $K_3(T)$  is defined by

$$\ell_t + 1 \leq K_3(T) := \min \{ \lceil T/4 \rceil + 1, n + 1 \}.$$

- **Length-update circuit for updating  $\ell_t$ .** We execute the length-update circuit only at step indices  $T$  that are multiples of four. This circuit acts on qubits indexed from  $\ell_t$  to  $(n + 3 - \ell_{r'})$ , and the corresponding two-sided active window is defined by

$$\begin{aligned} \ell_t &\geq k_4(T) := \max \left\{ \left\lceil \frac{T - 4(n + 2)}{4c - 4} \right\rceil, 1 \right\}, \\ n + 3 - \ell_{r'} &\leq K_4(T) := \min \{ T/4 + 3, n + 3 \}. \end{aligned}$$

- **Length-update circuit for updating  $\ell_{r'}$ .** Let  $\ell_t^*, \ell_{r'}^*$  denote the updated value of  $\ell_t, \ell_{r'}$  after the length update. This circuit acts on qubits indexed from  $\ell_t^* + 2$  to  $(n + 4 - \ell_{r'}^*)$ , and the corresponding two-sided active window is defined by

$$\begin{aligned} \ell_t^* + 2 &\geq k_5(T) := \lceil T/(4c) \rceil, \\ n + 4 - \ell_{r'}^* &\leq K_5(T) := \min \{ T/4 + 4, n + 3 \}. \end{aligned}$$

## 5 Explicit Quantum Circuit Construction and Resource Estimation

We adopt the resource-estimation methodology introduced by Roetteler et al. [RNSL17]. In Shor's algorithm for the ECDLP, the dominant quantum cost arises from the sequence of controlled elliptic-curve point additions performed in superposition. We consider the point additions in affine coordinates over the finite field  $\mathbb{F}_p$ , where  $p$  is an  $n$ -bit prime. At this level, point addition reduces to a fixed sequence of modular additions, subtractions, doublings, multiplications, squarings, and inversions. Among these operations, modular inversion typically dominates both the required circuit width and the Toffoli gate count.

## 5.1 Space complexity improvement from modular inversion

In [RNSL17], their implementation of controlled point addition requires

$$9n + 2\lceil \log_2 n \rceil + 10$$

logical qubits in total. Within this construction, the inversion subroutine itself uses

$$7n + 2\lceil \log_2 n \rceil + 9$$

logical qubits. The remaining qubits consist of a single global control qubit and two additional  $n$ -qubit registers that are used to store intermediate values during each inversion.

Subsequent work by Häner et al. [HJN<sup>+</sup>20] further optimized the trade-offs between Toffoli count, circuit depth, and width in point-addition circuits. Under a low-width design, they report a reduction in the number of logical qubits for a 256-bit curve from 2338 to 2124, together with substantial improvements in both  $T$ -count and  $T$ -depth.

Our contribution is orthogonal to these optimizations. Rather than exploring trade-offs between Toffoli count, circuit depth, and qubit width, we focus exclusively on reducing the qubit width required to implement modular inversion. We present a space-efficient and exact reversible modular inversion procedure based on the register-sharing technique originally proposed by Proos and Zalka [PZ03]. This approach reduces the qubit width of modular inversion to

$$3n + 4\lceil \log_2 n \rceil + 20,$$

which is also summarized in Table 6.

## 5.2 Asymptotic gate count for modular inversion

The leading term of the Toffoli/CNOT gate count arises from the implementation of location-controlled operations, which require  $O(n^2 \log_2 n)$  Toffoli/CNOT gates. Within the detailed circuit construction of these operations, the leading-order cost arises from arithmetic operations on the `Length` registers; the remaining components contribute only  $O(n^2)$  Toffoli/CNOT gates.

As shown in Appendix B, an  $\ell$ -bit quantum incrementer requires  $(2\ell - 2)$  Toffoli gates and  $(\ell + 2)$  CNOT gates. Using the step-dependent active window described in Section 4.3, we derive the asymptotic Toffoli gate count associated with each type of location-controlled operation. Recall that  $c = 1/\log_2\left(\frac{\sqrt{5}+1}{2}\right)$ .

- **Location-controlled addition/subtraction on  $r$ 's.** At step  $T$ , these operations consist of  $4(K_1(T) - k_1(T)) + O(1)$  quantum incrementers. The total Toffoli gate count is

$$2 \sum_{T=1}^{4\lceil cn \rceil} 8 \log_2 n (K_1(T) - k_1(T)) + O(n^2) = (32c + 8)n^2 \log_2 n + O(n^2).$$

- **Location-controlled swap.** At step  $T$ , these operations consist of  $(K_2(T) - k_2(T)) + O(1)$  quantum incrementers. The resulting Toffoli gate count is

$$\sum_{T=1}^{4\lceil cn \rceil} 2 \log_2 n (K_2(T) - k_2(T)) + O(n^2) = (4c + 1)n^2 \log_2 n + O(n^2).$$

- **Location-controlled addition/subtraction on  $t$ 's.** At step  $T$ , these operations consist of  $2(K_3(T) - k_3(T)) + O(1)$  quantum incrementers. The corresponding Toffoli gate count is

$$2 \sum_{T=1}^{4\lceil cn \rceil} 4 \log_2 n (K_3(T) - k_3(T)) + O(n^2) = (32c - 16)n^2 \log_2 n + O(n^2).$$

- **Length-update circuit for updating  $\ell_t$ .** We execute the length-update circuit only at step indices  $T$  that are multiples of four. At step  $T = 4T'$ , these operations consist of  $6(K_4(4T') - k_4(4T')) + O(1)$  quantum incrementers. The total Toffoli gate count is

$$\sum_{T'=1}^{\lceil cn \rceil} 12 \log_2 n (K_4(4T') - k_4(4T')) + O(n^2) = 6cn^2 \log_2 n + O(n^2).$$

- **Length-update circuit for updating  $\ell_{r'}$ .** We execute the length-update circuit only at step indices  $T$  that are multiples of four. At step  $T = 4T'$ , these operations consist of  $6(K_5(4T') - k_5(4T')) + O(1)$  quantum incrementers. The resulting Toffoli gate count is

$$\sum_{T'=1}^{\lceil cn \rceil} 12 \log_2 n (K_5(4T') - k_5(4T')) + O(n^2) = (6c - 6)n^2 \log_2 n + O(n^2).$$

Combining all contributions, the total number of Toffoli gates required by our modular inversion circuit grows asymptotically as

$$2(80c - 13)n^2 \log_2 n + O(n^2) \approx 204n^2 \log_2 n + O(n^2).$$

The asymptotical bound of CNOT gates required by our modular inversion circuit is therefore about  $102n^2 \log_2 n + O(n^2)$ .

### 5.3 Numerical experiments for modular inversion

All resource-estimation experiments were conducted on a Linux server equipped with an AMD EPYC 7302 processor (up to 3.0 GHz). Circuit generation and compilation were performed using IBM Qiskit. The constructed circuits were transpiled into a gate basis consisting of **CCX**, **CX**, and **X** gates, in order to obtain accurate Toffoli-gate and CNOT-gate counts.

Our implementation is built directly from the explicit circuit construction presented in Section 4. Following the analysis of the one-step modular-inversion circuit, we implemented each circuit component in Qiskit as an independent module, including the pre-shift and post-shift blocks, the location-controlled arithmetic and swap blocks, the phase-update logic, and the length-update circuits. These modules were then synthesized into full modular-inversion circuits by composing them according to the step schedule of Algorithm 3 and the corresponding step-dependent active windows.

The corresponding circuit implementation is included in our open-source codebase.<sup>2</sup> For each problem size  $n$ , we generated the full circuit instance up to the theoretical upper bound on the number of cycles

<sup>2</sup>GitHub repository: <https://github.com/ZeroWang030221/Space-Efficient-Quantum-Algorithm-for-Elliptic-Curve-Discrete-Logarithms-with-Resource-Estimation>

derived in this work, transpiled it into the **CCX**, **CX**, and **X** basis, and recorded the resulting gate counts. We report results for  $n \in \{64, 128, 160, 192, 224, 256, 384, 512\}$ . The numerical values are listed in Table 5.

It is noteworthy that our Toffoli gate count exceeds the CNOT count in Table 5. This ratio arises because most arithmetic sub-components are nested within two external control bits (Phase 1 and Phase 2 in Section 3.1) that transform internal CNOT gates to Toffoli gates. Additionally, our constant adders are optimized for increment operations, significantly reducing the CNOT overhead compared to standard constructions (see Appendix B for details).

$n$	Toffoli ( $\times 10^8$ )	CNOT ( $\times 10^8$ )
64	0.10	0.07
128	0.44	0.32
160	0.78	0.54
192	1.12	0.77
224	1.51	1.04
256	1.97	1.36
384	3.53	3.28
512	6.24	5.82

Table 5: Toffoli and CNOT gate counts for modular inversion circuits over  $n$ -bits prime fields.

#### 5.4 Resource Estimates for ECDLP

We next propagate the improvement of Section 5.2 from the modular-inversion subroutine to the full quantum circuit for solving the ECDLP. To keep the accounting uniform, we use only *Toffoli*-based cost estimates in this subsection. More precisely, we adopt the high-level affine-Weierstrass point-addition decomposition of [RNSL17, Figure 10] and [HJN<sup>+</sup>20, Figure 9], and evaluate all arithmetic components in Toffoli gates using the resource table of [RNSL17, Table 1].

**Controlled affine point addition.** As discussed in the preliminaries, given affine points  $P_1 = (x_1, y_1)$  and  $P_2 = (x_2, y_2)$  that are not inverse to each other, one computes

$$x_3 = \lambda^2 - x_1 - x_2, \quad y_3 = \lambda(x_1 - x_3) - y_1,$$

so that  $(x_3, y_3) = P_1 + P_2$ . The corresponding controlled circuit is shown schematically in Figure 10. Following [RNSL17, Figure 10] and [HJN<sup>+</sup>20, Figure 9], we count one such point addition as consisting of 4 modular divisions, 4 modular multiplications, 1 modular squaring, and a constant number of modular additions/subtractions/negations. The latter contribute only  $O(n \log_2 n)$  Toffoli gates in total and are therefore absorbed into the lower-order term.

Table 6 shows the modular-arithmetic summary table of [RNSL17, Table 1], but we (i) report only the **dbl/add** variants for multiplication/squaring to reduce space overhead, and (ii) replace **inv\_modp** by our inversion module. The non-inversion Toffoli counts are taken from [RNSL17].

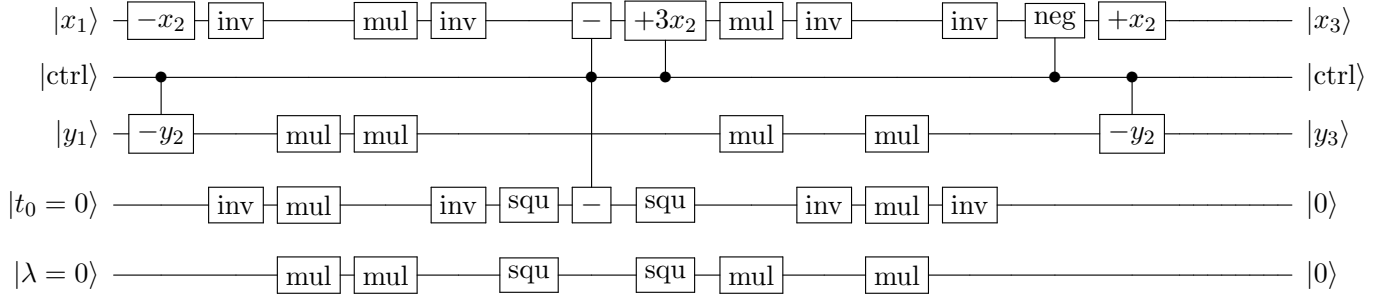


Figure 10: Schematic low-width controlled affine Weierstrass point-addition circuit, adapted from the construction of [RNSL17, Figure 10].

Modular arithmetic circuit	# of logical qubits		# Toffoli gates
	total	ancillas	
add_const_modp, sub_const_modp	$2n$	$n$	$16n \log_2(n) - 26.9n$
ctrl_add_const_modp, ctrl_sub_const_modp	$2n + 1$	$n$	$16n \log_2(n) - 26.9n$
ctrl_sub_modp	$2n + 4$	3	$16n \log_2(n) - 23.8n$
ctrl_neg_modp	$n + 3$	2	$8n \log_2(n) - 14.5n$
mul_modp (dbl/add)	$3n + 2$	2	$32n^2 \log_2(n) - 59.4n^2$
squ_modp (dbl/add)	$2n + 3$	3	$32n^2 \log_2(n) - 59.4n^2$
inv_modp ( <b>this work</b> )	$3n + 4\lceil \log_2(n) \rceil + O(1)$	$n + 4\lceil \log_2(n) \rceil + O(1)$	$204n^2 \log_2 n$

Table 6: Modular-arithmetic resource summary for affine point addition over  $\mathbb{F}_p$  with  $n$ -bit prime  $p$ . The first two rows use one/two clean ancillas and may additionally borrow dirty ancillas as in [RNSL17]. All other ancillas are assumed clean and are returned to  $|0\rangle$ . Non-inversion entries follow [RNSL17]; the inversion entry is replaced by our circuit.

Therefore, a single controlled affine point addition requires

$$(4 \cdot 204 + 4 \cdot 32 + 32)n^2 \log_2 n + O(n^2) = 976n^2 \log_2 n + O(n^2)$$

Toffoli gates.

**Resource estimates for Shor’s ECDLP circuit.** For the full ECDLP attack, we do not repeat the controlled point-addition circuit bit-by-bit for all  $2n$  control bits. Instead, we follow the signed-window technique of [HJN<sup>+</sup>20, Section 5.1]. Namely, we partition the  $2n$  control bits arising in the double-scalar multiplication into windows of size  $w$ , and implement each window by one signed windowed point addition.

In the signed-window construction, one of the  $w$  bits is used as a sign bit, while the remaining  $w - 1$  bits address a precomputed table of point multiples. As shown schematically in Fig. 10 of [HJN<sup>+</sup>20], one

such windowed point addition consists of the same dominant arithmetic core as a single affine Weierstrass point addition, together with six table look-ups and one modular negation. Since the dominant  $n^2 \log_2 n$  term in our Toffoli accounting comes from modular divisions, multiplications and squaring, replacing the classically known addend by a looked-up cache point affects only lower-order terms.

To obtain a clean asymptotic bound, we choose window size  $\omega = 2 \log_2 n$  to fit the signed windowed point addition. A sequential quantum look-up over a table of size  $2^{\omega-1}$  contributes  $O(2^\omega) = O(n^2)$  Toffoli gates, and hence the six look-ups together contribute only  $O(n^2)$  Toffoli gates. The full double-scalar multiplication now uses approximately  $2n/\omega$  such windows, so the dominant Toffoli count of Shor’s ECDLP circuit becomes

$$\frac{2n}{\omega}(976n^2 \log n + O(n^2)) = 976n^3 + O\left(\frac{n^3}{\log_2 n}\right).$$

Finally, we note that compression techniques and multi-run tradeoffs [Eke19] could potentially yield further improvements to the constant factors in our overall resource estimates.

## Acknowledgments

ZY, ZW, YS and TL are supported by the National Natural Science Foundation of China (Grant Numbers 62372006 and 92365117).

## References

- [AMMR13] Matthew Amy, Dmitri Maslov, Michele Mosca, and Martin Roetteler. A meet-in-the-middle algorithm for fast synthesis of depth-optimal quantum circuits. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, 32(6):818–830, 2013. <https://doi.org/10.1109/TCAD.2013.2244643>.
- [BBvHL20] Gustavo Banegas, Daniel J. Bernstein, Iggy van Hoof, and Tanja Lange. Concrete quantum cryptanalysis of binary elliptic curves. *Cryptology ePrint Archive*, 2020. <https://eprint.iacr.org/2020/1296>.
- [BD20] Elaine Barker and Quynh Dang. NIST special publication 800-57 part 1, revision 5, recommendation for key management: Part 1–general. *NIST, Technical Report*, page 171, 2020.
- [BWBG<sup>+</sup>06] Simon Blake-Wilson, Nelson Bolyard, Vipul Gupta, Chris Hawk, and Bodo Moeller. Elliptic curve cryptography (ECC) cipher suites for transport layer security (TLS), 2006. <https://www.rfc-editor.org/rfc/rfc4492.html>.
- [BWQ99] Simon Blake-Wilson and M. Qu. Standards for efficient cryptography (sec) 2: Recommended elliptic curve domain parameters. *Certicom Research, Oct*, page 25, 1999.

- [BZG<sup>+</sup>26] Ryan Babbush, Adam Zalcman, Craig Gidney, Michael Broughton, Tanuj Khattar, Hartmut Neven, Thiago Bergamaschi, Justin Drake, and Dan Boneh. Securing elliptic curve cryptocurrencies against quantum vulnerabilities: Resource estimates and mitigations, 2026. arXiv:[2603.28846](https://arxiv.org/abs/2603.28846)
- [CDKM04] Steven A. Cuccaro, Thomas G. Draper, Samuel A. Kutin, and David Petrie Moulton. A new quantum ripple-carry addition circuit. *arXiv preprint*, 2004. arXiv:[quant-ph/0410184](https://arxiv.org/abs/quant-ph/0410184)
- [CFS25] Clémence Chevignard, Pierre-Alain Fouque, and André Schrottenloher. Reducing the number of qubits in quantum factoring. In *Annual International Cryptology Conference*, pages 384–415. Springer, 2025. [https://doi.org/10.1007/978-3-032-01878-6\\_13](https://doi.org/10.1007/978-3-032-01878-6_13).
- [CFS26] Clémence Chevignard, Pierre-Alain Fouque, and André Schrottenloher. Reducing the number of qubits in quantum discrete logarithms on elliptic curves. *Cryptology ePrint Archive*, Paper 2026/280, 2026. <https://eprint.iacr.org/2026/280>.
- [CvD10] Andrew M. Childs and Wim van Dam. Quantum algorithms for algebraic problems. *Reviews of Modern Physics*, 82(1):1–52, 2010. <https://doi.org/10.1103/RevModPhys.82.1>.
- [DH76] Whitfield Diffie and Martin E. Hellman. New directions in cryptography. *IEEE Transactions on Information Theory*, 22(6), 1976. <https://doi.org/10.1145/3549993.3550007>.
- [Eke19] Martin Ekerå. Revisiting Shor’s quantum algorithm for computing general discrete logarithms, 2019. arXiv:[1905.09084](https://arxiv.org/abs/1905.09084)
- [ElG85] Taher ElGamal. A public key cryptosystem and a signature scheme based on discrete logarithms. *IEEE Transactions on Information Theory*, 31(4):469–472, 1985. <https://doi.org/10.1109/TIT.1985.1057074>.
- [FMCM12] Austin G. Fowler, Matteo Mariantoni, John M. Martinis, and Andrew N. Cleland. Surface codes: Towards practical large-scale quantum computation. *Physical Review A*, 86(3):032324, 2012. <https://doi.org/10.1103/PhysRevA.86.032324>.
- [GE21] Craig Gidney and Martin Ekerå. How to factor 2048 bit RSA integers in 8 hours using 20 million noisy qubits. *Quantum*, 5:433, 2021. <https://doi.org/10.22331/q-2021-04-15-433>.
- [GG16] Steven D. Galbraith and Pierrick Gaudry. Recent progress on the elliptic curve discrete logarithm problem. *Designs, Codes and Cryptography*, 78(1):51–72, 2016. <https://doi.org/10.1007/s10623-015-0146-7>.
- [Gid25] Craig Gidney. How to factor 2048 bit RSA integers with less than a million noisy qubits. *arXiv preprint*, 2025. arXiv:[2505.15917](https://arxiv.org/abs/2505.15917)
- [GN96] Robert B. Griffiths and Chi-Sheng Niu. Semiclassical Fourier transform for quantum computation. *Physical Review Letters*, 76(17):3228, 1996. <https://doi.org/10.1103/PhysRevLett.76.3228>.

- [GYCM25] Quan Gu, Han Ye, Junjie Chen, and Xiongfeng Ma. Resource analysis of Shor’s elliptic curve algorithm with an improved quantum adder on a two-dimensional lattice. *arXiv preprint arXiv:2510.23212*, 2025.
- [Has36] Helmut Hasse. Zur theorie der abstrakten elliptischen Funktionenkörper II. Automorphismen und Meromorphismen. Das Additionstheorem. *Journal für die reine und angewandte Mathematik*, 1936. <https://doi.org/10.1515/crll.1936.175.69>.
- [HJN<sup>+</sup>20] Thomas Häner, Samuel Jaques, Michael Naehrig, Martin Roetteler, and Mathias Soeken. Improved quantum circuits for elliptic curve discrete logarithms. In *International Conference on Post-quantum Cryptography*, pages 425–444. Springer, 2020. [https://doi.org/10.1007/978-3-030-44223-1\\_23](https://doi.org/10.1007/978-3-030-44223-1_23).
- [HRS17] Thomas Häner, Martin Roetteler, and Krysta M. Svore. Factoring using  $2n + 2$  qubits with Toffoli based modular multiplication. *Quantum Info. Comput.*, 17(7–8):673–684, June 2017. <https://dl.acm.org/doi/abs/10.5555/3179553.3179560>.
- [JKL<sup>+</sup>22] Kyungbae Jang, Wonwoong Kim, Sejin Lim, Yeajun Kang, Yujin Yang, and Hwajeong Seo. Optimized implementation of quantum binary field multiplication with Toffoli depth one. In *International Conference on Information Security Applications*, pages 251–264. Springer, 2022. [https://doi.org/10.1007/978-3-031-25659-2\\_18](https://doi.org/10.1007/978-3-031-25659-2_18).
- [JMV01] Don Johnson, Alfred Menezes, and Scott Vanstone. The elliptic curve digital signature algorithm (ECDSA). *International Journal of Information Security*, 1(1):36–63, 2001. <https://doi.org/10.1007/s102070100002>.
- [JSB<sup>+</sup>25] Kyungbae Jang, Vikas Srivastava, Anubhab Baksi, Santanu Sarkar, and Hwajeong Seo. New quantum cryptanalysis of binary elliptic curves (extended version). *Cryptology ePrint Archive*, 2025. <https://eprint.iacr.org/2025/017>.
- [KJW<sup>+</sup>26] Hyunji Kim, Kyungbae Jang, Siyi Wang, Anubhab Baksi, Gyeongju Song, Hwajeong Seo, and Anupam Chattopadhyay. New quantum circuits for ECDLP: Breaking prime elliptic curve cryptography in minutes. *Cryptology ePrint Archive*, Paper 2026/106, 2026. <https://eprint.iacr.org/2026/106>.
- [KMRVvK25] Gregory D Kahanamoku-Meyer, Seyoon Ragavan, Vinod Vaikuntanathan, and Katherine van Kirk. The Jacobi factoring circuit: Quantum factoring with near-linear gates and sublinear space and depth. In *Proceedings of the 57th Annual ACM Symposium on Theory of Computing*, pages 1496–1507, 2025. <https://doi.org/10.1145/3717823.3718273>.
- [Kob87] Neal Koblitz. Elliptic curve cryptosystems. *Mathematics of Computation*, 48(177):203–209, 1987. <https://doi.org/10.1090/S0025-5718-1987-0866109-5>.
- [KSG<sup>+</sup>25] Tanuj Khattar, Noah Shetty, Craig Gidney, Adam Zalcman, Noureldin Yosri, Dmitri Maslov, Ryan Babbush, and Stephen P. Jordan. Verifiable quantum advantage via optimized DQI circuits, 2025. arXiv:2510.10967

- [Mil85] Victor S. Miller. Use of elliptic curves in cryptography. In *Conference on the Theory and Application of Cryptographic Techniques*, pages 417–426. Springer, 1985. [https://doi.org/10.1007/3-540-39799-X\\_31](https://doi.org/10.1007/3-540-39799-X_31).
- [NB08] Satoshi Nakamoto and A. Bitcoin. A peer-to-peer electronic cash system. *Bitcoin.–URL: https://bitcoin.org/bitcoin.pdf*, 4(2):15, 2008.
- [NC10] Michael A. Nielsen and Isaac L. Chuang. *Quantum computation and quantum information*. Cambridge University Press, 2010.
- [PWLK22] Dedy Septono Catur Putranto, Rini Wisnu Wardhani, Harashta Tatimma Larasati, and Howon Kim. Another concrete quantum cryptanalysis of binary elliptic curves. *Cryptology ePrint Archive*, 2022. <https://eprint.iacr.org/2022/501>.
- [PZ03] John Proos and Christof Zalka. Shor’s discrete logarithm quantum algorithm for elliptic curves. *Quantum Info. Comput.*, 3(4):317–344, July 2003. <https://dl.acm.org/doi/abs/10.5555/2011528.2011531>.
- [Reg25] Oded Regev. An efficient quantum factoring algorithm. *Journal of the ACM*, 72(1):1–13, 2025. <https://doi.org/10.1145/3708471>.
- [RNSL17] Martin Roetteler, Michael Naehrig, Krysta M. Svore, and Kristin Lauter. Quantum resource estimates for computing elliptic curve discrete logarithms. In *International Conference on the Theory and Application of Cryptology and Information Security*, pages 241–270. Springer, 2017. [https://doi.org/10.1007/978-3-319-70697-9\\_9](https://doi.org/10.1007/978-3-319-70697-9_9).
- [RSA78] Ronald L. Rivest, Adi Shamir, and Leonard Adleman. A method for obtaining digital signatures and public-key cryptosystems. *Communications of the ACM*, 21(2):120–126, 1978. <https://doi.org/10.1145/359340.359342>.
- [RV24] Seyoon Ragavan and Vinod Vaikuntanathan. Space-efficient and noise-robust quantum factoring. In *Annual International Cryptology Conference*, pages 107–140. Springer, 2024. [https://doi.org/10.1007/978-3-031-68391-6\\_4](https://doi.org/10.1007/978-3-031-68391-6_4).
- [SG09] Douglas Stebila and Jon Green. Elliptic curve algorithm integration in the secure shell transport layer, 2009. <https://www.rfc-editor.org/rfc/rfc5656>.
- [Sho94] Peter W. Shor. Algorithms for quantum computation: discrete logarithms and factoring. In *Proceedings 35th Annual Symposium on Foundations of Computer Science*, pages 124–134. IEEE, 1994. <https://doi.org/10.1109/SFCS.1994.365700>.
- [TT23] Ren Taguchi and Atsushi Takayasu. Concrete quantum cryptanalysis of binary elliptic curves via addition chain. In *Cryptographers’ Track at the RSA Conference*, pages 57–83. Springer, 2023. [https://doi.org/10.1007/978-3-031-30872-7\\_3](https://doi.org/10.1007/978-3-031-30872-7_3).

# A Proof Details

## A.1 Bounds on the total number of steps

Suppose that after  $k$  iterations of the Extended Euclidean Algorithm, we obtain  $r_{k-1} = 1$  and  $r_k = 0$ , with intermediate quotients  $q_1, q_2, \dots, q_{k-1}$ , where  $q_i = \lfloor r_{i-1}/r_i \rfloor$  for  $i = 1, 2, \dots, k-1$ . Then the total number of steps required in our four-phase algorithm can be expressed as

$$N = 4 \sum_{i=1}^{k-1} (\lfloor \log_2 q_i \rfloor + 1).$$

The lower bound of  $N$  can be derived directly. Since  $r_{i-1} = q_i r_i + r_{i+1} < (q_i + 1)r_i$ , it follows that

$$N \geq 4 \sum_{i=1}^{k-1} \log_2(q_i + 1) > 4 \sum_{i=1}^{k-1} \log_2 \frac{r_{i-1}}{r_i} = 4 \log_2 p \geq 4(n-1).$$

Because  $N$  must be a multiple of 4, we conclude that  $N \geq 4n$ .

To derive the upper bound of  $N$ , we take a complementary viewpoint. Instead of fixing  $p$  and computing  $N$ , we fix  $N$  and seek the smallest possible value of  $p$  as  $k$  and the quotient sequence  $\{q_i\}_{i=1}^{k-1}$  vary. Note that  $p = r_0$  can be reconstructed recursively from the sequence defined by  $r_k = 0$ ,  $r_{k-1} = 1$ , and  $r_{i-1} = r_{i+1} + q_i r_i$ ,  $i = k-1, k-2, \dots, 1$ . To minimize  $p$  under this recurrence, we apply the following sequence of adjustment steps, keeping  $N = 4 \sum_{i=1}^{k-1} (b_i + 1)$  fixed:

- We first adjust all quotients to powers of two, i.e.,  $q_i = 2^{b_i}$  with  $b_i = \lfloor \log_2 q_i \rfloor$ . This modification is justified because reducing any quotient strictly decreases the corresponding sequence  $r_{i-1}, \dots, r_0$ .
- For any  $i = 1, 2, \dots, k-2$ , if  $b_i \geq 2$  for  $i = 1$  and  $b_i \geq 1$  for  $i > 1$ , we can split the EEA iteration with quotient  $q_i = 2^{b_i}$  into two successive iterations with quotients  $q_{i,1} = 1$  and  $q_{i,2} = 2^{b_i-1}$ . The updated value of  $r_{i-1}$  is then

$$r'_{i-1} = r_i + q_{i,1}(r_{i+1} + q_{i,2}r_i) = r_{i+1} + (2^{b_i-1} + 1)r_i \leq r_{i+1} + 2^{b_i}r_i = r_{i-1},$$

implying that the modified sequence yields a smaller  $p$ . The condition  $b_1 \geq 2$  when  $i = 1$  is required since the algorithm assumes  $x < p/2$ .

- If  $b_{k-1} \geq 2$ , we further refine the final iteration with  $q_{k-1} = 2^{b_{k-1}}$  by splitting it into two iterations with quotients  $q_{k-1,1} = 2$  and  $q_{k-1,2} = 2^{b_{k-1}-2}$ . This adjustment differs from the previous one because  $r_{k-2}$  must remain greater than 1. The updated value of  $r_{k-2}$  becomes

$$r'_{k-2} = 1 + q_{k-1,1} \cdot q_{k-1,2} = 1 + 2^{b_{k-1}-1} < 2^{b_{k-1}} = r_{k-2},$$

showing once again that the adjustment leads to a smaller  $p$  for the same total number of steps.

After applying all possible adjustments, we obtain a quotient sequence of form  $\{q_i\} = \{2, 1, 1, \dots, 1, 2\}$  with length  $k-1 = N/4 - 2$ . The corresponding sequence of  $r_i$  satisfies

$$r_{k-1} = 1, \quad r_{k-2} = 2, \quad r_{i-1} = r_{i+1} + r_i \text{ for } i = k-2, \dots, 2, \quad \text{and } r_0 = r_2 + 2r_1.$$

This recurrence defines a Fibonacci sequence with  $r_{k-i} = F_{i+1}$  for  $i = 1, 2, \dots, k-1$ , and the minimal possible value of  $p$  is thus  $p = r_0 = F_{k-1} + 2F_k = F_{k+2} = F_{N/4+1}$ . Together with the condition  $2^{n-1} \leq p < 2^n$ , we obtain

$$\frac{1}{\sqrt{5}} \left( \frac{\sqrt{5}+1}{2} \right)^{N/4+1} \leq F_{N/4+1} + 1 \leq p + 1 \leq 2^n.$$

Hence,

$$N \leq 4 \left\lceil c \left( n + \log_2 \sqrt{5} \right) - 1 \right\rceil \leq 4 \lceil cn \rceil,$$

where  $c = 1/\log_2 \left( \frac{\sqrt{5}+1}{2} \right)$ .

## A.2 Step-dependent active windows

Fix an input  $x$ , let  $(q_1, \dots, q_{k-1})$  denote the quotient sequence produced by EEA, and define  $b_i := \lfloor \log_2 q_i \rfloor$  for each iteration  $i$ . Under the four-phase schedule, each EEA iteration  $i$  is expanded into  $4(b_i + 1)$  steps. The total number of steps is  $N = 4 \sum_{i=1}^{k-1} (b_i + 1) \leq N_{\max} := 4 \lceil cn \rceil$ , where  $c = 1/\log_2 \left( \frac{\sqrt{5}+1}{2} \right)$  (see Appendix A.1).

For a global step index  $T \in \{1, 2, \dots, N_{\max}\}$ , let  $j = j(x, T)$  denote the index of the EEA iteration that contains step  $T$ , and let  $u = u(x, T)$  denote the position of  $T$  within that iteration. More precisely, the pair  $(j(x, T), u(x, T))$  is uniquely determined by the conditions

$$\sum_{i=1}^{j-1} 4(b_i + 1) < T \leq \sum_{i=1}^j 4(b_i + 1), \quad u = T - \sum_{i=1}^{j-1} 4(b_i + 1).$$

The bit-length of the current quotient  $\ell_q(x, T)$  depends deterministically on indices  $(j, u)$ :

$$\ell_q(x, T) = \begin{cases} 0 & u(x, T) \in (0, b_j + 1] \cup (3(b_j + 1), 4(b_j + 1)], \\ u(x, T) - (b_j + 1) & u(x, T) \in (b_j + 1, 2(b_j + 1)], \\ 3(b_j + 1) - u & u(x, T) \in (2(b_j + 1), 3(b_j + 1)]. \end{cases} \quad (2)$$

We next state a lemma that characterizes the maximal possible value of  $t_j$ , conditioned on the total number of steps  $N_j$  taken before reaching the  $j$ -th iteration of EEA. The proof follows exactly the same adjustment argument as in Appendix A.1, and is therefore omitted.

**Lemma A.1.** *Suppose that  $N_j = \sum_{i=1}^{j-1} 4(b_i + 1)$  is fixed. Then, over all possible EEA iteration indices  $j$  and all admissible quotient sequences  $(q_1, \dots, q_{j-1})$ , we have  $t_j \geq F_{N_j/4+1}$ , and consequently,*

$$\lfloor \log_2 t_j \rfloor + 1 \geq \log_2 \left( \frac{\sqrt{5}+1}{2} \right) \cdot \frac{N_j}{4}.$$

Here,  $\{F_k\}_{k \geq 0}$  denotes the Fibonacci sequence  $F_0 = 0, F_1 = 1$ , and  $F_{k+2} = F_{k+1} + F_k$  for all  $k \geq 0$ .

We then provide the detailed proofs of the bounds stated in Section 4.3 in the remainder of this subsection. Recall that  $c = 1/\log_2 \left( \frac{\sqrt{5}+1}{2} \right)$ .

**Location-controlled addition/subtraction on  $r$ 's.** First, observe that  $t_j q_j < t_{j+1} < p$ , which implies  $\ell_t + b_j \leq n + 1$ . Since a location-controlled addition/subtraction on  $r$ 's is only activated in Phase 1 and 2, i.e.  $0 < u \leq 2(b_j + 1)$ , we then analyze the claimed bound by considering two cases.

- **Case 1.** Suppose that  $u \leq b_j + 1$ . In this case, we have  $\ell_q = 0$ . By Lemma A.1, it follows that

$$\ell_t \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - (n + 2 - \ell_t)}{4},$$

$$\text{hence } \ell_t + \ell_q = \ell_t \geq \frac{T - n - 2}{4c - 1}.$$

- **Case 2.** Suppose that  $b_j + 1 < u \leq 2(b_j + 1)$ . Then  $\ell_q = u - (b_j + 1)$ , and we obtain that

$$\ell_t + \ell_q \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} + (u - b_j - 1).$$

The right-hand side is minimized when  $u = b_j + 1$ , in which case the expression reduces to that of Case 1.

Combining the two cases, we conclude that  $\ell_t + \ell_q + 2 \geq \max \left\{ \left\lceil \frac{T - n - 2}{4c - 1} \right\rceil, 1 \right\} + 2$ .

**Location-controlled swaps.** For the lower bound, a location-controlled swap is only activated in Phase 2 and 3, i.e.  $b_j + 1 < u \leq 3(b_j + 1)$ , we then analyze the claimed lower bound by considering two cases.

- **Case 1.** Suppose that  $b_j + 1 < u \leq 2(b_j + 1)$ . In this case, we also have  $\ell_t + \ell_q \geq \frac{T - n - 2}{4c - 1}$ .
- **Case 2.** Suppose that  $2(b_j + 1) < u \leq 3(b_j + 1)$ . In this case, we have  $\ell_q = 3(b_j + 1) - u$ . By Lemma A.1, it follows that

$$\ell_t \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - 3(n + 2 - \ell_t)}{4},$$

$$\text{hence } \ell_t + \ell_q \geq \ell_t \geq \frac{T - 3(n + 2)}{4c - 3}.$$

Combining the two cases, we conclude that  $\ell_t + \ell_q + 1 \geq \max \left\{ \left\lceil \frac{T - 3(n + 2)}{4c - 3} \right\rceil, 1 \right\} + 1$ .

For the upper bound, recall the recurrence relation of the EEA on the  $t$ -sequence, that is  $t_{i+1} = t_{i-1} + q_i t_i < (q_i + 1)t_i \leq 2^{b_i+1} t_i$ . By iterating this inequality, we obtain that

$$t = t_j \leq \prod_{i=1}^{j-1} 2^{b_i+1} = 2^{(T-u)/4}, \quad \text{and then } \ell_t \leq (T - u)/4 + 1.$$

By Equation (2), we know that  $\ell_q \leq u/2$ . Hence,

$$\ell_t + \ell_q + 1 \leq \lfloor (T - u)/4 + u/2 + 2 \rfloor = \lfloor (T + u)/4 \rfloor + 2 \leq \lfloor T/2 \rfloor + 2.$$

Finally, since the `Work1` register stores a value  $r \geq 1$ , we conclude that  $\ell_t + \ell_q + 1 \leq n + 2$ .

**Location-controlled addition/subtraction on  $t$ 's.** As we proved before, We have that  $\ell_t + 1 \leq \lfloor (T - u)/4 \rfloor + 2 \leq \lceil T/4 \rceil + 1$ . By the constraint that  $t \leq p < 2^n$ , we also obtain that  $\ell_t + 1 \leq n + 1$ .

**Length-update circuit.** For the lower bound  $k_4(T)$ , the length-update circuit is activated only at the end of an EEA iteration, namely when  $u = 4(b_j + 1)$ . By Lemma A.1, we have

$$\ell_t \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - u}{4} \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T - 4(n + 2 - \ell_t)}{4},$$

which implies  $\ell_t \geq \frac{T - 4(n + 2)}{4c - 4}$ .

For the lower bound  $k_5(T)$ , Lemma A.1 directly yields

$$\ell_t^* \geq \log_2 \left( \frac{\sqrt{5} + 1}{2} \right) \cdot \frac{T}{4} = \frac{T}{4c}.$$

For the upper bound  $K_5(T)$ , recall the recurrence relation of the EEA on the  $r$ -sequence,  $r_{i-1} = r_{i+1} + q_i r_i < (q_i + 1)r_i \leq 2^{b_i+1} r_i$ . By iterating this inequality, we obtain

$$p/r_{j+1} \leq \prod_{i=1}^j 2^{b_i+1} = 2^{T/4}.$$

It follows that  $n + 4 - \ell_{r'} < n + 4 - \log_2 r_{j+1} \leq T/4 + n + 4 - \log_2 p \leq T/4 + 5$ , and hence  $n + 4 - \ell_{r'} \leq T/4 + 4$ .

For the upper bound  $K_4(T)$ , we similarly have  $n + 3 - \ell_{r'} \leq n + 3 - \ell_{r'}^* \leq T/4 + 3$ .

## B Optimization of Quantum Constant Adder

We adopt the linear-depth ripple-carry adder of Cuccaro et al. [CDKM04], which computes carries in a forward sweep and erases them in a backward sweep using two elementary reversible blocks: an in-place majority gate MAJ and an ‘‘unmajority-and-add’’ gate UMA. The MAJ and UMA blocks can both be implemented by two CNOT gates and one Toffoli gate.

Let  $a = \sum_{i=0}^{n-1} a_i 2^i$  be an  $n$ -bit addend and  $b = \sum_{i=0}^{n-1} b_i 2^i$  be an  $n$ -bit quantum integer. We denote the carry bits by  $c_0, c_1, \dots, c_n$  with  $c_0 = 0$ . The classical carry recursion is

$$c_{i+1} = \text{MAJ}(a_i, b_i, c_i), \quad s_i = a_i \oplus b_i \oplus c_i,$$

where  $\text{MAJ}(x, y, z)$  is the majority function. The Cuccaro construction computes  $c_1, \dots, c_n$  by chaining MAJ blocks, and then uncomputes carries while writing the sum bits by chaining UMA blocks.

**Gate count for the baseline.** Each bit position contributes one MAJ block and one UMA block. With MAJ realized as (2CNOT + 1Toffoli) and UMA (2-CNOT version) realized as (2CNOT + 1Toffoli), the resulting ripple-carry constant adder uses

$$\#\text{Toffoli} = 2n, \quad \#\text{CNOT} = 4n + 1,$$

where the additional +1 CNOT accounts for the final XOR into the most significant sum bit in the standard MAJ/UMA chaining pattern (matching the circuit structure in the ripple-carry diagram).

**Specialize to the increment.** We now specialize the constant adder to the increment operation  $b \mapsto b + 1$ . In this case, the addend satisfies  $a_0 = 1, a_i = 0$  for  $i = 1, 2, \dots, n - 1$ . This bit pattern simplifies both the carry recursion and the sum expressions, which in turn allows systematic cancellation of CNOT gates whose controls are zeros.

- For  $i \geq 1$  we have  $a_i = 0$ , hence

$$c_{i+1} = \text{MAJ}(0, b_i, c_i) = b_i c_i. \quad (3)$$

Operationally, any CNOT in the MAJ template whose control is  $a_i$  becomes trivial and can be removed. What remains is exactly one Toffoli gate to compute  $c_{i+1}$  from  $(b_i, c_i)$  (written into the designated carry location), with no CNOTs for these stages.

- For the least significant bit,  $a_0 = 1$  and  $c_0 = 0$ . The first carry is

$$c_1 = \text{MAJ}(1, b_0, 0) = b_0,$$

so the initialization of the carry chain can be implemented with only Clifford operations (a single CNOT that copies  $b_0$  into the carry wire and two NOT gates).

- For  $i \geq 1$ , since  $a_i = 0$ , the sum bit reduces to  $s_i = b_i \oplus c_i$ . In the backward sweep, UMA simultaneously (i) erases  $c_{i+1}$  and (ii) writes  $s_i$  into the target bit line. With  $a_i = 0$ , the CNOTs in the 2-CNOT UMA template that are controlled by  $a_i$  again vanish. The stage can therefore be implemented using: (i) one CNOT to compute  $b_i \leftarrow b_i \oplus c_i$  (thereby writing  $s_i$ ), and (ii) one Toffoli to uncompute the carry contribution corresponding to Equation (3).
- The least significant bit can similarly be performed using a single CNOT that copies  $b_0$  into the carry wire and one NOT gate.

Collecting the above simplifications yields the following count.

**Gate count for the incrementer.** Let  $b$  be an  $n$ -bit quantum integer and consider the constant increment map  $b \mapsto b + 1$  implemented by specializing the Cuccaro ripple-carry adder with the 2-CNOT UMA construction. Then the circuit can be compiled to use

$$\#\text{Toffoli} = 2n - 2, \quad \#\text{CNOT} = n + 2,$$

up to Clifford-only single-qubit corrections (NOT gates).