

Resource analysis of Shor’s elliptic curve algorithm with an improved quantum adder on a two-dimensional lattice

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Quantum computers have the potential to break classical cryptographic systems by efficiently solving problems such as the elliptic curve discrete logarithm problem using Shor’s algorithm. While resource estimates for factoring-based cryptanalysis are well established, comparable evaluations for Shor’s elliptic curve algorithm under realistic architectural constraints remain limited. In this work, we propose a carry-lookahead quantum adder that achieves Toffoli depth $\log n + \log \log n + O(1)$ with only $O(n)$ ancillas, matching state-of-the-art performance in depth while avoiding the prohibitive $O(n \log n)$ space overhead of existing approaches. Importantly, our design is naturally compatible with the two-dimensional nearest-neighbor architectures and introduce only a constant-factor overhead. Further, we perform a **comprehensive resource analysis of Shor’s elliptic curve algorithm on two-dimensional lattices using the improved adder**. By leveraging dynamic circuit techniques with mid-circuit measurements and classically controlled operations, our construction incorporates the windowed method, Montgomery representation, and quantum tables, and substantially reduces the overhead of long-range gates. For cryptographically relevant parameters, we provide precise resource estimates. In particular, **breaking the NIST P-256 curve, which underlies most modern public-key infrastructures and the security of Bitcoin, requires about 4300 logical qubits** and logical Toffoli fidelity about 10^{-9} . These results establish new benchmarks for efficient quantum arithmetic and provide concrete guidance toward the experimental realization of Shor’s elliptic curve algorithm.

I. INTRODUCTION

Quantum algorithms, such as Shor’s algorithm [1], Grover’s search [2], the HHL algorithm [3], and Hamiltonian simulation [4], offer potential speedups over their classical counterparts. Tremendous efforts have been devoted to their experimental realization across a variety of physical platforms [5–7]. However, noise and decoherence make demonstrating quantum advantage with noisy intermediate-scale quantum (NISQ) devices challenging [8]. As recent works suggest that classically hard problem instances remain beyond the reach of NISQ algorithms [9, 10], it becomes essential to explore the precise resource requirements for implementing large-scale quantum algorithms under realistic hardware assumptions.

One of the most prominent cryptographic applications of quantum algorithms is Shor’s solution to the elliptic curve discrete logarithm problem. The hardness of this problem underpins widely deployed cryptographic systems such as key agreement [11], digital signatures [12, 13], and pseudorandom generators [14], with notable implementations including the NIST P-256, P-384, and P-521 curves [15]. In particular, Bitcoin relies on the secp256k1 elliptic curve to ensure the security of its transactions [16]. An efficient algorithm for solving the elliptic-curve discrete logarithm problem would put at risk any bitcoins whose public keys have been revealed, as well as funds in transactions that have been broadcast to the network but not yet confirmed on the blockchain, which may worth trillions of dollars [17]. The security of systems ranging from internet protocols to blockchain technologies relies directly on the conjectured classical intractability of this problem [18]. Although believed to be hard classically, Shor’s algorithm can solve the elliptic curve discrete logarithm problem in polynomial time [1, 19]. While the resource demands for Shor’s factoring algorithm have been extensively analyzed [20–24], systematic studies for Shor’s elliptic curve algorithm remain comparatively limited [25, 26].

Any realistic analysis must account for architectural constraints. Leading quantum platforms such as superconducting qubits [5] and topological qubits [20] are naturally restricted to two-dimensional (2D) nearest-neighbor layouts. This geometry strikes a balance between scalability, fabrication feasibility, and compatibility with error correction, but it also imposes significant routing and depth overheads for nonlocal gates. Since Shor’s elliptic curve algorithm relies heavily on modular arithmetic, these architectural constraints make the efficiency of arithmetic subroutines, especially quantum adders, central to any realistic resource estimate.

At the core of modular arithmetic, quantum adders serve as one of the most fundamental primitives in quantum computing. Optimizing the trade-off between circuit depth and ancilla overhead is especially crucial for the

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NISQ devices, where the number of available qubits is limited and circuit depth is constrained by decoherence and uncorrectable noise. A shallower adder not only reduces execution time but also mitigates cumulative noise, while minimizing ancilla qubits enhances scalability and physical realizability on current hardware platforms. Ripple-carry adders achieve linear Toffoli depth with minimal ancilla overhead [27, 28], whereas carry-lookahead adders attain logarithmic depth at the cost of linear or larger ancillary space. As key references for evaluating the trade-off between depth and ancilla usage, the most well-known carry-lookahead adder achieves a depth of $2 \log n + O(1)$ with $O(n)$ ancillas [29], while the best known depth of $\log n + 1$ has recently been obtained at the expense of $O(n \log n)$ ancillas [30].

In this work, we propose a new carry-lookahead quantum adder that achieves Toffoli depth $\log n + \log \log n + O(1)$ with only $O(n)$ ancillas, achieving state-of-the-art performance of depth while avoiding the prohibitive space overhead of prior designs. Our construction is naturally compatible with two-dimensional nearest-neighbor architectures with only constant-factor overhead in this setting. A comparison of the resource costs of our in-place adder with previous works is shown in Table I.

TABLE I: Comparison of our in-place quantum adder with previous works

Adder	qubit number	Toffoli depth	Toffoli number
Brent-Kung tree [29] ¹	$5n + O(1)$	$4 \log n + O(1)$	$10n + O(1)$
Sklansky tree [30] ²	$\frac{1}{2}n \log n + 3n + O(1)$	$2 \log n + O(1)$	$2n \log n + 2n + O(1)$
Our work	$6n + O(1)$	$2 \log n + 2 \log \log n + O(1)$	$14n + O(1)$

¹ In the original paper, it costs $4n + O(1)$ bits. However, in order to achieve a dynamic Toffoli gate with T -depth 1, one additional column is needed.

² We made some quick improvements on the qubit numbers compared to the original paper.

Building on this improved adder, we present a comprehensive resource analysis of Shor’s elliptic curve algorithm compiled for two-dimensional nearest-neighbor lattices. Our construction integrates several key algorithmic ingredients, including the windowed trick [26], Montgomery representation [31], and quantum tables [32], while leveraging dynamic circuit techniques to reduce the cost of nonlocal operations. Dynamic circuits, incorporating mid-circuit measurements, feedforward, and classically controlled operations, enable polynomial overheads for long-range gates to be traded for constant spatial overhead. Beyond their foundational role in fault-tolerant quantum error correction [33, 34], dynamic circuits have also demonstrated broad utility in state preparation [35, 36], measurement-based quantum computing [37, 38], and gate compilation [39]. By exploiting this capability, our analysis achieves dramatically reduced depth in 2D layout. We provide explicit circuit designs and quantify resource costs in terms of circuit depth, qubit number, and logical gate counts. We summarize the exact costs for input sizes of 25, 32, 192, 256, 384, and 521, and also the leading-order terms for general n in Table II. A figure illustrating the relation between Toffoli number, Toffoli depth and input size is shown in Fig. 1. Specifically, for cryptographically relevant security levels, we estimate that solving a single instance of the NIST P-256 curve, whose hardness underlies the security of Bitcoin and other major blockchain systems, would require at least 4300 logical qubits and Toffoli-gate fidelity better than 10^{-9} .

TABLE II: Resource estimation of Shor’s algorithm for the elliptic curve discrete logarithm problem. The last row shows the leading terms.

Input size	qubit number	CNOT depth	CNOT count	Toffoli depth	Toffoli count
25	425	2.12×10^5	3.55×10^6	1.17×10^5	1.84×10^6
32	544	3.69×10^5	7.86×10^6	1.68×10^5	2.94×10^6
192	3264	1.11×10^7	1.30×10^9	5.95×10^6	5.32×10^8
256	4352	1.89×10^7	2.89×10^9	1.09×10^7	1.33×10^9
384	7528	4.41×10^7	9.99×10^9	2.47×10^7	4.20×10^9
521	8857	8.58×10^7	2.67×10^{10}	4.44×10^7	9.51×10^9
n	$17n$	$96n^2 + 240 \frac{n^2}{\log \log n}$	$80 \frac{n^3}{\log \log n} + 1490 \frac{n^3}{\log n}$	$112n^2 + 80 \frac{n^2}{\log \log n}$	$1144 \frac{n^3}{\log n} + 280 \frac{n^3}{\log n \log \log n}$

This paper is organized as follows. Section II reviews the necessary background, including the elliptic curve discrete logarithm problem, Shor’s elliptic curve algorithm, the 2D layout model, and the concept of dynamic circuits. Section III presents our improved quantum adder and analyzes its performance. Section IV provides a detailed resource analysis of Shor’s elliptic curve algorithm on a 2D lattice. Section V discusses the implications of our results and outlines possible directions for future research.

The appendices provide additional technical details. Appendix A describes the construction of the Toffoli gate, a

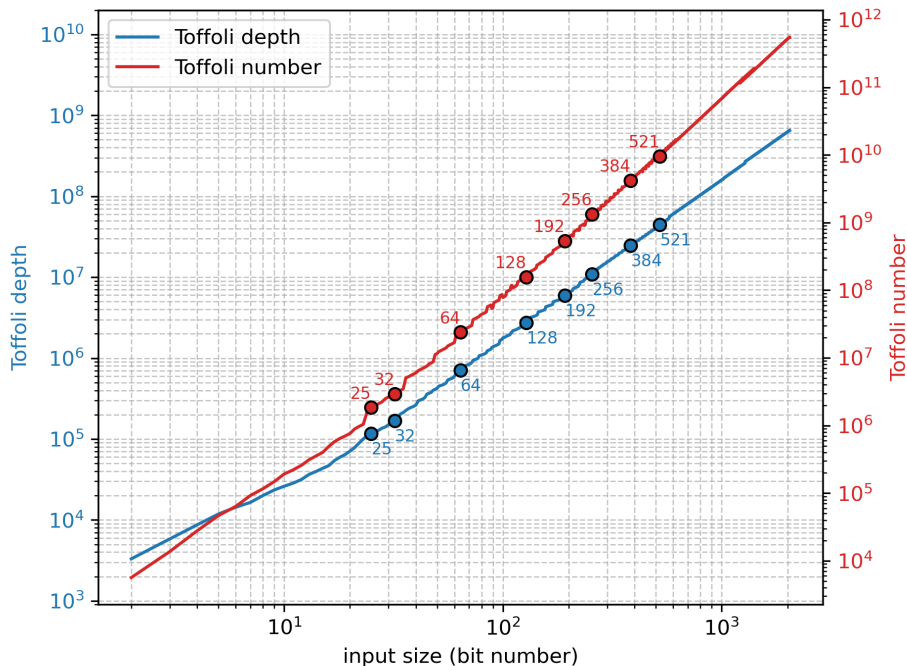


FIG. 1: The relationship between the Toffoli depth, Toffoli number, and the input size n (i.e., the bit length of the elliptic curve). These metrics are evaluated by simulating our circuit for n values from 2 to 2048. Minor fluctuations in the Toffoli number appear when the window size increases by one.

key component of our circuit. Appendix B reviews two early designs of carry-lookahead adders that form the basis of our improved adder. Appendix C details the implementation of several important arithmetic subroutines used in our analysis. Appendix D lists the explicit calculations of the resource costs. Appendix E presents the construction of other essential circuit components. Finally, Appendix F demonstrates the implementation of our circuit on a single-layer layout as an alternative to the bi-layer design used in the main text.

II. PRELIMINARIES

In this section, we briefly introduce preliminary knowledge, including the formal definition of elliptic curve discrete logarithm problem, Shor’s algorithm to solve it, the layout of a 2D system and the concept and usage of dynamic circuits.

A. Elliptic curve discrete logarithm problem

We only provide a concise overview of the elliptic curve discrete logarithm problem here, and leave the details of elliptic curve digital signature algorithms to Ref. [13]. An elliptic curve can be defined over finite fields \mathbb{F}_p , where p is a prime. All subsequent arithmetic operations are thus performed within the finite field \mathbb{F}_p : the operations “+”, “−”, and “ \times ” are understood modulo p , and the division “ a/b ” is defined by $a \times b^{-1}$, where b^{-1} denotes the multiplicative inverse of b in \mathbb{F}_p .

Formally, an elliptic curve in short Weierstrass form E over \mathbb{F}_p is defined as the set of points $P = (x, y)$ satisfying the constraint $y^2 = x^3 + ax + b$, where constants $a, b \in \mathbb{F}_p$ should fulfill the non-singularity condition $4a^3 + 27b^3 \neq 0$. To construct an Abelian group based on the points on E , an identity element O and the point addition should be defined. Define the point O as the point at infinity, which cannot be represented in \mathbb{F}_p^2 . The addition operation on points of the elliptic curve E is then defined as follows. Let $P_1, P_2 \in E$ and $P_3 = P_1 + P_2$. If either $P_1 = O$ or $P_2 = O$, the addition is simply defined by $P_3 = P_2$ or $P_3 = P_1$, respectively. If both P_1 and P_2 are distinct from O , we write their coordinates explicitly as $P_1(x_1, y_1)$ and $P_2(x_2, y_2)$. If $x_1 = x_2$ and $y_1 = -y_2$, we let $P_3 = O$ and say that P_2 is

the inverse of P_1 , denoted $P_1 = -P_2$. Otherwise, $P_3(x_3, y_3)$ can be computed via the following equation

$$(x_3, y_3) = (\lambda^2 - x_1 - x_2, -y_2 - \lambda(x_3 - x_2)), \quad (1)$$

where the slope

$$\lambda = \begin{cases} \frac{y_1 - y_2}{x_1 - x_2}, & \text{if } P_1 \neq P_2, \\ \frac{3x_1^2 + a}{2y_1}, & \text{if } P_1 = P_2. \end{cases} \quad (2)$$

We still use \mathbf{E} to represent the Abelian group. The scalar multiplication between $m \in \mathbb{F}_p$ and $P \in \mathbf{E}$ is defined naturally by repeated addition as

$$mP = \underbrace{P + P + \cdots + P}_m \quad (3)$$

when $m \neq 0$, and $0P = O$.

Suppose the cardinality of the group $|\mathbf{E}|$ has a large prime factor q . One can find a cyclic subgroup of \mathbf{E} of order q , denoted as $\{O, G, 2G, \dots, (q-1)G\}$ with $qG = O$. Specifically, $|\mathbf{E}| = q$ typically endows the elliptic curve with advantageous cryptographic properties. However, this constraint is not necessary for the analysis presented here.

In elliptic curve digital signature algorithms, each user possesses a private key $d \in [1, q-1]$ and a corresponding public key defined as $Q = dG$ [13]. The security of these algorithms relies on the computational difficulty of deriving the private key d from the known generator point G and the public key Q . That is, given two points $G, Q \in \mathbf{E}$, there is no known classical polynomial-time algorithm for computing $d \in \mathbb{F}_p$ such that $dG = Q$. Successfully solving for d would compromise the encryption scheme by enabling an adversary to forge signatures. This computationally challenging task is widely recognized as the elliptic curve discrete logarithm problem.

B. Shor's elliptic curve Algorithm

Although certain specialized classical algorithms can efficiently attack elliptic curves with particular structural properties, there currently exists no general classical algorithm capable of solving the elliptic curve discrete logarithm problem with a time complexity better than $O(\sqrt{q})$ [13]. Consequently, the elliptic curve discrete logarithm problem is widely considered unbreakable by classical computers.

However, Shor's quantum algorithm provides a general and efficient quantum solution to the elliptic curve discrete logarithm problem. Its procedure can be summarized as follows [40].

$$\begin{aligned}
& |0\rangle |0\rangle |0\rangle && \text{initial state} \\
\rightarrow & \frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle |y\rangle |0\rangle && \text{apply H gates on the first two registers} \\
\rightarrow & \frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle |y\rangle |xG + yQ\rangle && \text{apply controlled point addition} \\
= & \frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle |y\rangle |(x + yd)G\rangle \\
= & \frac{1}{2^n \sqrt{q}} \sum_{l=0}^{q-1} \sum_{x,y=0}^{2^n-1} e^{2\pi i(x+yd)l/q} |x\rangle |y\rangle |\psi(l)\rangle \\
= & \frac{1}{2^n \sqrt{q}} \sum_{l=0}^{q-1} \left(\sum_{x=0}^{2^n-1} e^{2\pi ixl/q} |x\rangle \right) \left(\sum_{y=0}^{2^n-1} e^{2\pi idly/q} |y\rangle \right) |\psi(l)\rangle \\
\rightarrow & \frac{1}{\sqrt{q}} \sum_{l=0}^{q-1} |\widetilde{l/q}\rangle |\widetilde{dl/q}\rangle |\psi(l)\rangle && \text{apply inverse QFT on the first two registers} \\
\rightarrow & |\widetilde{l/q}\rangle |\widetilde{dl/q}\rangle && \text{measure the first two registers}
\end{aligned} \quad (4)$$

Here, the equation in the fifth line is based on the quantum Fourier transform (QFT), where $|\psi(l)\rangle$ is defined as $|\psi(l)\rangle = \frac{1}{\sqrt{q}} \sum_{j=0}^{q-1} e^{-2\pi i l j/q} |jG\rangle$. After applying the inverse quantum Fourier transform, the state $\sum_{x=0}^{2^n-1} e^{2\pi i l x/q} |x\rangle$ is transformed to $|\widetilde{l/q}\rangle$, which closely approximates the computational basis state $|l/q\rangle$. $|\widetilde{dl/q}\rangle$ is obtained and near to $|dl/q\rangle$ in the same way. Therefore, if we measure the first two registers on the computational basis, the outcome of the second register should be d times the outcome of the first register with high probability. A simple diversity will give d and the problem can be solved in polynomial time and space of $n = \Theta(\log d)$.

The main computational primitives in Shor’s algorithm are controlled point addition and QFT. While the circuit of QFT is well established [1], there needs additional design for realizing controlled point addition $|x\rangle |P_1\rangle |P_2\rangle \mapsto |x\rangle |P_1\rangle |P_2 + xP_1\rangle$. Note that the core issue is to design the point addition $|P_1\rangle |P_2\rangle \mapsto |P_1\rangle |P_2 + P_1\rangle$, since the control operation can be realized by adding a quantum control on each gate in the original circuit. Each point $|P\rangle$ should be represented as $|x\rangle |y\rangle$. One can use the classical algorithm for point addition based on Eq. (1) and replace the corresponding classical operations with reversible quantum operations. Here, “reversible” means that we cannot erase any information during the computation process. As shown in Algorithm 1, we need quantum circuits for modular addition $|x_1\rangle |x_2\rangle \mapsto |x_1 - x_2\rangle |x_2\rangle$, modular multiplication $|x\rangle |y\rangle |\lambda\rangle \mapsto |x\rangle |y \oplus \lambda \cdot x\rangle |\lambda\rangle$, and modular division $|x\rangle |y\rangle |\lambda\rangle \mapsto |x\rangle |y\rangle |\lambda \oplus \frac{y}{x}\rangle$, which will be discussed in Appendix C.

Algorithm 1: (reversible) classical algorithm for point addition [25]

Input : x_1, x_2, y_1, y_2

Output: x_3, y_3

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 $x \leftarrow x_1, y \leftarrow y_1$  ;
 $x \leftarrow x - x_2, y \leftarrow y - y_2$  ;
 $\lambda \leftarrow \frac{y}{x}$  ;
 $y \leftarrow y \oplus (\lambda \cdot x)$  ;
 $x \leftarrow x + 3x_2 - \lambda^2$  ;
 $y \leftarrow \lambda \cdot x$  ;
 $\lambda \leftarrow \lambda \oplus \frac{y}{x}$  ;
 $x \leftarrow x_2 - x, y \leftarrow y - y_2$  ;
return  $x, y$ 

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//  $x = x_1 - x_2, y = y_1 - y_2$ 
//  $\lambda = \frac{y_1 - y_2}{x_1 - x_2}$ 
//  $\oplus$  for bit-wise XOR;  $y = 0$ 
//  $x = x_1 + 2x_2 - \lambda^2 = x_2 - x_3$ 
//  $y = \lambda \cdot (x_2 - x_3) = y_2 + y_3$ 
//  $\oplus$  for bit-wise XOR;  $\lambda = 0$ 
//  $x = x_3, y = y_3$ 

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C. 2D Layout

Two-dimensional (2D) qubit layouts are widely favored in quantum computing, as they offer the minimal geometry required for implementing high-threshold topological codes while remaining compatible with leading physical platforms, most notably superconducting architectures. In this work, we introduce two 2D layouts tailored for Shor’s algorithm, each comprising $17n$ qubits. The first is a single-layer $n \times 17$ lattice, referred to as the “single-layer layout”, and the second is a bi-layer $n \times 9 \times 2$ lattice, referred to as the “bi-layer layout”. Among them, $2n$ qubits are to store the result of point addition, $13n$ qubits are for intermediate computations, and the other $2n$ qubits are ancillas. For algorithmic convenience, we permit a slight extension in the column size, such as $n + \log n$, rather than fixing it exactly at n . The two layouts are illustrated in Fig. 2. The bi-layer layout enables more efficient execution of nearest-neighbor gates, whereas the single-layer layout requires gate teleportation or swap operations, incurring only constant overhead. In the main text, we focus on circuit design based on the bi-layer layout, while additional details of the single-layer layout are provided in Appendix F.

To manipulate n -qubit registers (e.g., applying arithmetic operations such as addition or multiplication), we organize the qubits vertically into columns containing n qubits each. Columns of idle qubits, that is, qubits in state $|0\rangle$, can be employed by dynamic circuits to facilitate the implementation of circuits requiring long-range gate interactions.

Throughout our analysis, certain multi-qubit gates inevitably act on qubits that are not nearest neighbors. To quantify this aspect, we define the gate interaction distance as the maximum Manhattan distance between any two qubits involved in a gate on the lattice, where the Manhattan distance between two qubits located at positions (x_1, y_1) and (x_2, y_2) is given by $|x_1 - x_2| + |y_1 - y_2|$. For practical quantum computing implementations, gate interaction distances of gate bricks used for compilation should remain constant, since it only introduces a constant overhead to decompose them into nearest-neighbor two-qubit gates. While we retain the multi-qubit representation for clarity and conciseness, the gate interaction distance provides a direct measure of the resource overhead incurred when compiling abstract gates into hardware-compatible nearest-neighbor interactions, and is thus an essential consideration for practical implementations.

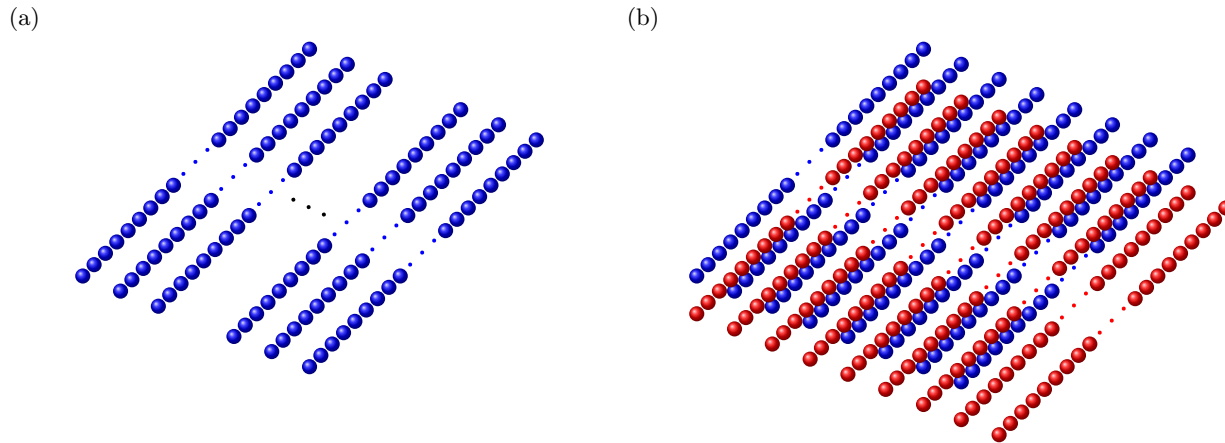


FIG. 2: Two diagrams illustrating the qubit layout. (a) The diagram for the single-layer layout, each ball representing a qubit, and each line consists of n qubits. (b) The diagram for the bi-layer layout, each ball representing a qubit, and each line consists of n qubits. Blue balls stand for the qubits in the upper layer, red balls stand for those in the lower layer.

D. Dynamic Circuits

Dynamic quantum circuits, which integrate unitary gates, mid-circuit measurements, classical post-processing of measurement outcomes, and classically controlled unitary operations conditioned on the results of classical computing, offer computational capabilities beyond those of purely unitary circuits. They have been shown to provide advantages in quantum state preparation [35, 36, 41, 42] as well as in computational tasks [37–39]. A key feature of dynamic circuits is the ability to trade temporal complexity for spatial complexity, which can be accommodated by idle ancillary qubits. Leveraging dynamic circuits, it is possible to implement long-range quantum gates and generate long-range entangled states with substantially reduced depth, even under nearest-neighbor constraints. In this work, we focus on two fundamental dynamic circuits: the long-range Toffoli gate and unbounded GHZ-state generation [43], which we discuss in detail below.

Suppose we wish to implement a long-range Toffoli gate on three target qubits arranged along the same chain. Since data qubits cannot serve as ancillas or be directly measured during the process, we introduce an adjacent chain of ancillary qubits, each initialized to $|0\rangle$. As illustrated in Figs. 3a and 3c, long-range CNOTs, which are enabled by dynamic circuits, can be combined to realize the desired long-range Toffoli gate. The explicit circuit construction is provided in Figs. 3b and 3d. During the protocol, every ancilla qubit is measured once and reset to $|0\rangle$, allowing their reuse in subsequent dynamic circuits.

Another essential dynamic-circuit primitive in our circuit is unbounded GHZ state generation, which achieves the generalized quantum state “copying” operation:

$$a_0 |\psi_0\rangle |0\rangle + a_1 |\psi_1\rangle |1\rangle \mapsto a_0 |\psi_0\rangle |0\rangle^{\otimes n} + a_1 |\psi_1\rangle |1\rangle^{\otimes n}. \quad (5)$$

The preparation of such states with dynamic circuits of depth 6 and $n - 1$ ancillary qubits is well established; a representative implementation is shown in Fig. 4a [43].

Since the global phase is uniformly shared among all qubits in a GHZ state, the choice of control qubit in a controlled operation is irrelevant. Consequently, when multiple controlled gates share the same control qubit, one can first prepare a sufficiently large GHZ state and assign different qubits within it as individual controls, enabling all controlled gates to be executed in parallel, as illustrated in Fig. 4b. To recycle the ancillary qubits, any $n - 1$ qubits of the GHZ state are measured in the X basis, and an appropriate corrective operation (\mathbb{I} or Z) is applied to the remaining qubit depending on the measurement outcomes. On a two-dimensional lattice, this procedure can still be realized with constant-depth local gates and efficient classical post-processing, provided the ancillary qubits are placed in a column adjacent to the data qubits.

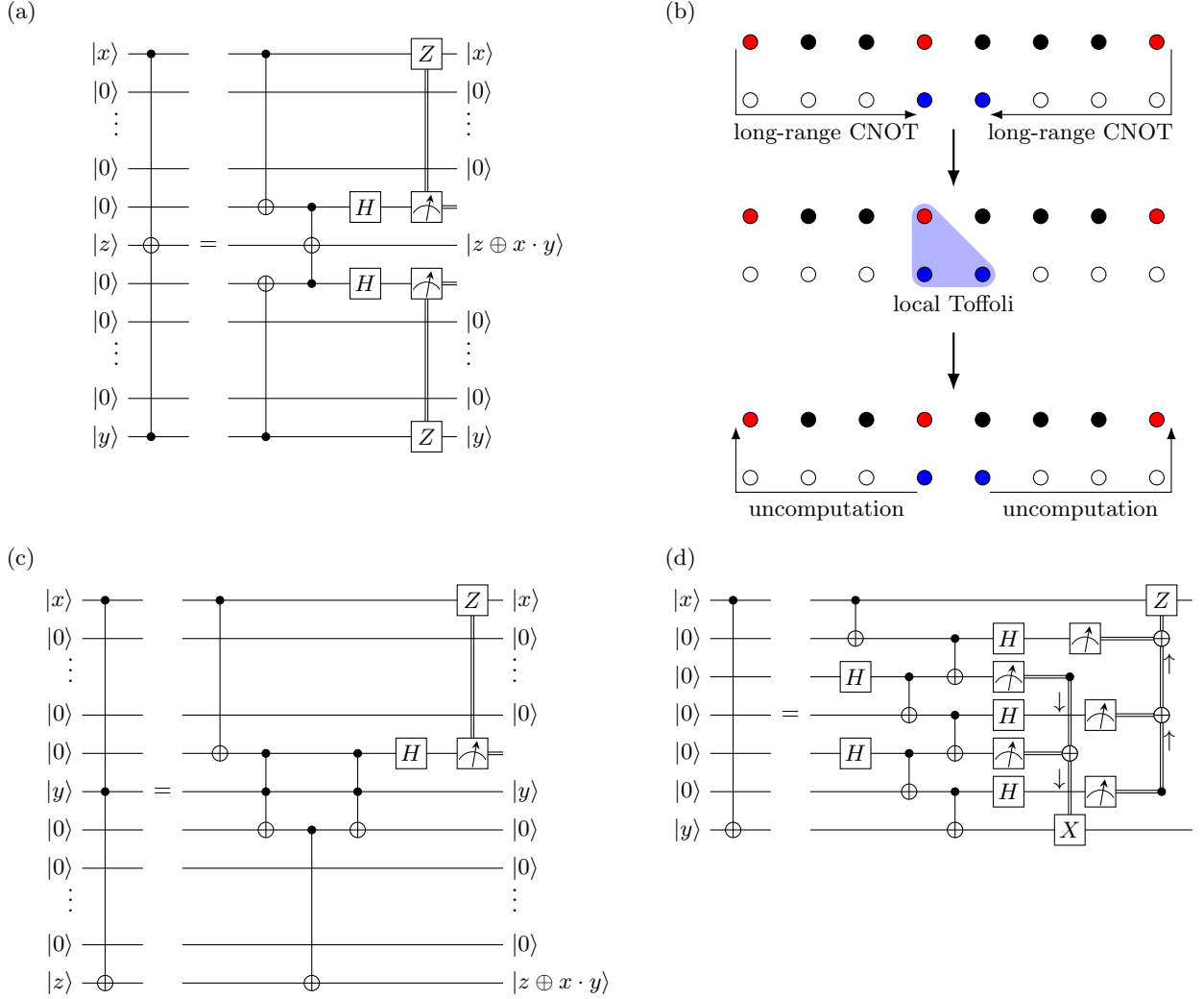


FIG. 3: Implementation of the long-range Toffoli gate using dynamic circuits. (a) An example of the circuit for implementing a long-range Toffoli gate with the output qubit in the middle. (b) The layout of ancillary qubits for the circuit in (a). We use red circles to represent the data qubits to implement Toffoli, black circles to represent the unused data qubits, white circles to represent the ancillary qubits initialized in $|0\rangle$, and blue circles to represent ancillas storing intermediate data. (c) An example of the circuit for implementing the long-range Toffoli gate with the output qubit on the edge. Notably, the second Toffoli gate is used for uncomputing the ancillary qubit, which can be designed with zero T -depth, as explained in Appendix A. Therefore, the two circuits shown by (a) and (c) have the same T -depth. (d) An example of implementing a long-range CNOT using dynamic circuit with a depth of 6.

III. IMPROVED QUANTUM ADDER

Efficient quantum addition is a fundamental building block for implementing arithmetic-intensive algorithms such as Shor's factoring and discrete logarithm algorithms. The performance of quantum adders directly impacts both the time and space complexity of these algorithms, since addition operations dominate the arithmetic subroutines. Improving the depth of quantum adders reduces overall circuit runtime and mitigates decoherence, while reducing the ancillary qubit overhead is critical for scalability on near-term and fault-tolerant architectures. Consequently, the design of quantum adders that simultaneously optimize time and space resources plays a central role in advancing the practical feasibility of large-scale quantum algorithms.

The classical adder computes the summation of two n -bit numbers x and y . The quantum adder implements a corresponding unitary U that produces $|s\rangle = |x + y\rangle$ given $|x\rangle|y\rangle$. Typically, there are two types of quantum adders: the out-place adder $U|x\rangle|y\rangle|0\rangle = |x\rangle|y\rangle|x + y\rangle$ and the in-place adder $U|x\rangle|y\rangle = |x\rangle|x + y\rangle$. We will only discuss

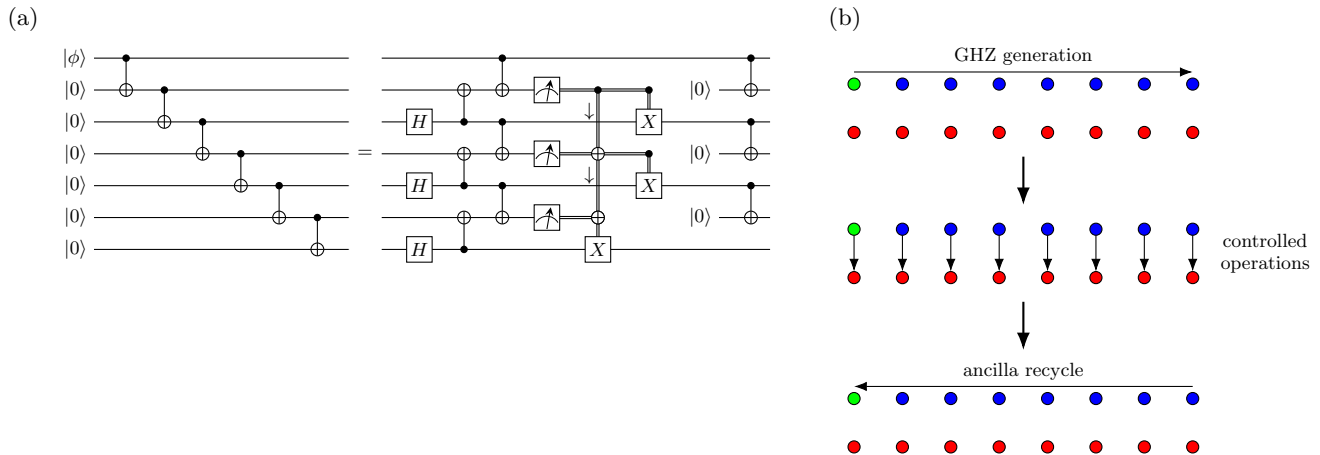


FIG. 4: Implementation of GHZ state generation. (a) Two equivalent circuits for implementing GHZ state generation. (b) Implement parallel controlled gates using GHZ state generation. We use red circles to represent the data qubits to implement controlled gates, green circles to represent the control qubit, and blue circles to represent ancillas storing intermediate data.

in-place adder in the main text and leave the discussion of out-place adder and other variants at Appendix E3. Our adder design is based on reversible classical adders, whose essential task is to compute the carry bits. Let x_i and y_i denote the i -th bits of x and y respectively, and let c_i denote the i -th carry bit. The final sum bits can be obtained in parallel given the carry bits as $s_i = x_i \oplus y_i \oplus c_i$.

Naively, the carry bits can be computed using a recursion equation $c_i = x_i y_i + x_i c_{i-1} + y_i c_{i-1}$. However, a direct implementation requires circuit depth $O(n)$, since the information from the data bits is propagated sequentially. In contrast, parallelization can be exploited to reduce the depth. By pre-processing the input bits x and y , one can enable parallel evaluation of carry bits, which is precisely the idea underlying classical carry-lookahead adders. To this end, the propagation state $p[i, j]$ and generation state $g[i, j]$ is defined by the recursion equations

$$\begin{aligned} p[i, j] &= p[i, k] \cdot p[k, j], \\ g[i, j] &= g[i, k] \oplus (p[i, k] \cdot g[k, j]). \end{aligned} \quad (6)$$

for $i < k < j$. The initial values give $p[i, i+1] = x_i \oplus y_i$ and $g[i, i+1] = x_i \cdot y_i$, and the carry bits are given by $c_j = g[0, j]$. The problem of solving the former recursion equation is known as “prefix sum problem” [44]. Solving this problem is the key part of designing quantum adder.

Various classical parallel prefix sum algorithms provide different trade-offs between time and space, which directly influence the design of quantum adders. The most well-known quantum carry-lookahead adder [29] computes the carry bits using a Brent-Kung tree [45], achieving depth $2 \log n + O(1)$ with $O(n)$ ancillas. By contrast, a more recent carry-lookahead construction based on the Sklansky tree [30, 46] reduces the depth to $\log n + 1$ but at the expense of $O(n \log n)$ ancillas. In this section, we introduce an improved carry-lookahead quantum adder that achieves Toffoli depth $\log n + \log \log n + O(1)$ with only $O(n)$ ancillas, thereby combining the advantages of both approaches.

A. Carry Bit Computing

Before introducing our algorithm for carry bit computing, we briefly introduce two previous methods [29, 30]. Intuitively, Draper’s method [29] utilizes a Brent-Kung tree structure [45], computing the value corresponding to the qubits located at the positions of powers of two in the first $\log n$ steps, and compute the other values in the remaining $\log n$ steps. Wang’s method [30], on the other hand, employs a Sklansky tree [46], updating the value of all qubits whose i -th bit of their locations are 1 at the i -th step. A demonstration of these two methods is shown in Fig. 5a and 5b, and the details of them can be found in Appendix B.

Our construction combines the advantages of Brent-Kung and Sklansky style carry-lookahead schemes within a windowed framework. The n qubits are partitioned into $m = \lceil n/k \rceil$ blocks of size $k = \lfloor \log n \rfloor$ (with the final block truncated if necessary). In the “block phase”, each k -qubit block is processed in parallel using a Brent-Kung tree to compute $p[ik, ik+j]$ and $g[ik, ik+j]$ for $0 \leq i < m$ and $1 \leq j \leq k$. In the “inter-block phase”, the block outputs

$p[ik, (i+1)k]$ and $g[ik, (i+1)k]$ are combined using a Sklansky tree, yielding the higher-level carries $g[0, ik]$. In the merge phase, these intermediate results are integrated with the block-level values to obtain $g[0, ik+j]$. Finally, all auxiliary values are uncomputed. The full procedure is summarized in Algorithm 2, and a schematic illustration is provided in Fig. 5c.

Algorithm 2: our algorithm for computing carry bits.

```

Function ComputeCarryOur( $P_0; G; P_1, P_2, a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $n$ -qubit  $G$  storing  $g[i-1, i]$ ;  $n$ -qubit ancilla  $P_1$ ,  $n$ -qubit ancilla  $P_2$ ,  $n$ -qubit
           ancilla  $a$ , all initialized to 0.
  Output:  $P_0, P_1, P_2, a$  remains the same;  $G$  holds carry bits  $c_i = g[0, i]$ .
1   $k \leftarrow \lfloor \log n \rfloor, m \leftarrow \lceil \frac{n}{k} \rceil$ ;
2  for  $i \leftarrow 0, \dots, m-1$  do
3    ComputeCarryDraperPGCompute( $P_0[ik, (i+1)k]; G[ik, (i+1)k]; P_1[ik, (i+1)k], P_2[ik, (i+1)k]; a[2ik, 2(i+1)k]$ );
    // set  $P_1[ik+j], G[ik+j]$  to  $p[ik, ik+j], g[ik, ik+j]$ 
4  ComputeCarryWang( $\{P_1[k], P_1[2k], \dots, P_1[n]\}; \{G_1[k], G_1[2k], \dots, G_1[n]\}; a$ ); // set  $G[ik]$  to  $g[0, ik]$ 
5  for  $i \leftarrow 0, \dots, m-1$  do
6    for  $j \leftarrow 1, \dots, \min\{k, n-ik\}$  do
7       $G[ik+j] \oplus= G[ik] \cdot P_1[ik+j]$ ; // set  $G[ik+j]$  to  $g[0, ik+j]$ 
8  for  $i \leftarrow 0, \dots, m-1$  do
9    ComputeCarryDraperPUncompute( $P_0[ik, (i+1)k]; P_1[ik, (i+1)k], P_2[ik, (i+1)k]; a[ik, (i+1)k]$ ); // recover
     $P_1, P_2$  to 0

```

We now analyze the resource cost of the proposed method, where “ \approx ” indicates that only leading terms are retained. Here, we use “I-O qubits” to denote the qubits served as both input and output qubits, which are not counted in “input qubits” or “output qubits”. In the block phase, the circuit uses n input qubits, $2n$ output qubits, n I-O qubits, and n ancillas. The Toffoli and CNOT depths are $\approx 2 \log k \approx 2 \log \log n$, and the Toffoli and CNOT counts are $\approx 4n$. In the inter-block phase, the circuit requires m inputs, m I-O qubits, and $\frac{1}{2}m \log m + m \approx \frac{1}{2}n$ ancillas, with Toffoli and CNOT depths $\approx \log m \approx \log n - \log \log n$ and gate counts $\approx m \log m \approx n - n \frac{\log \log n}{\log n}$. In the merge phase, $k-1$ copies of $G[ik]$ are prepared for each block using GHZ-state generation, costing $m \cdot \frac{3}{2}(k-1)$ CNOT gates with depth 3 and $(n-m)$ ancillas. The subsequent Toffoli gates are executed simultaneously, requiring an additional $(n-m)$ ancillas (two per Toffoli gate), after which the GHZ states are uncomputed at no extra Toffoli or CNOT cost. Thus, the merge phase uses $2(n-m)$ ancillas in total. This ancilla cost can be reduced to $\frac{2(n-m)}{k}$ at the expense of increasing the Toffoli depth to k . In this work, we allocate n ancillas for the merge phase, achieving Toffoli depth two. Overall, the construction involves n input qubits, n I-O qubits, and $3n$ ancillas, for a total of $5n$ qubits. The circuit depth and gate numbers are given by

$$\begin{aligned}
\text{Toffoli depth} &= \lfloor \log k \rfloor + \left\lceil \log \frac{2k}{3} \right\rceil + \lceil \log m \rceil + 1 = \log n + \log \log n + O(1), \\
\text{Toffoli number} &= m \cdot (4k - 2w(k) - 2 \lfloor \log k \rfloor - 2) + 2 \sum_{i=0}^{m-1} w(i) + n - m = 6n + O(1), \\
\text{CNOT depth} &= \lfloor \log k \rfloor + \left\lceil \log \frac{2k}{3} \right\rceil + 2 + \lceil \log m \rceil + 1 + 1 = \log n + \log \log n + O(1), \\
\text{CNOT number} &= m \cdot (4k - 2w(k) - 2 \lfloor \log k \rfloor - 2) + 2 \sum_{i=0}^{m-1} w(i) + m \cdot \frac{3}{2}(k-1) = \frac{13}{2}n + O(1),
\end{aligned} \tag{7}$$

where $w(n) = n - \sum_{i=1}^{\infty} \lfloor \frac{n}{2^i} \rfloor$ is the number of “1”s in the binary representation of n .

In conclusion, we obtain a quantum carry-bit computation algorithm with Toffoli depth $(1 + o(1)) \log n$ and only linear ancilla overhead, representing the best known trade-off to date. Building on the carry-bit construction, the in-place quantum adder is straightforward following the framework of [29], while the out-of-place variant and other extensions are described in Appendix E3.

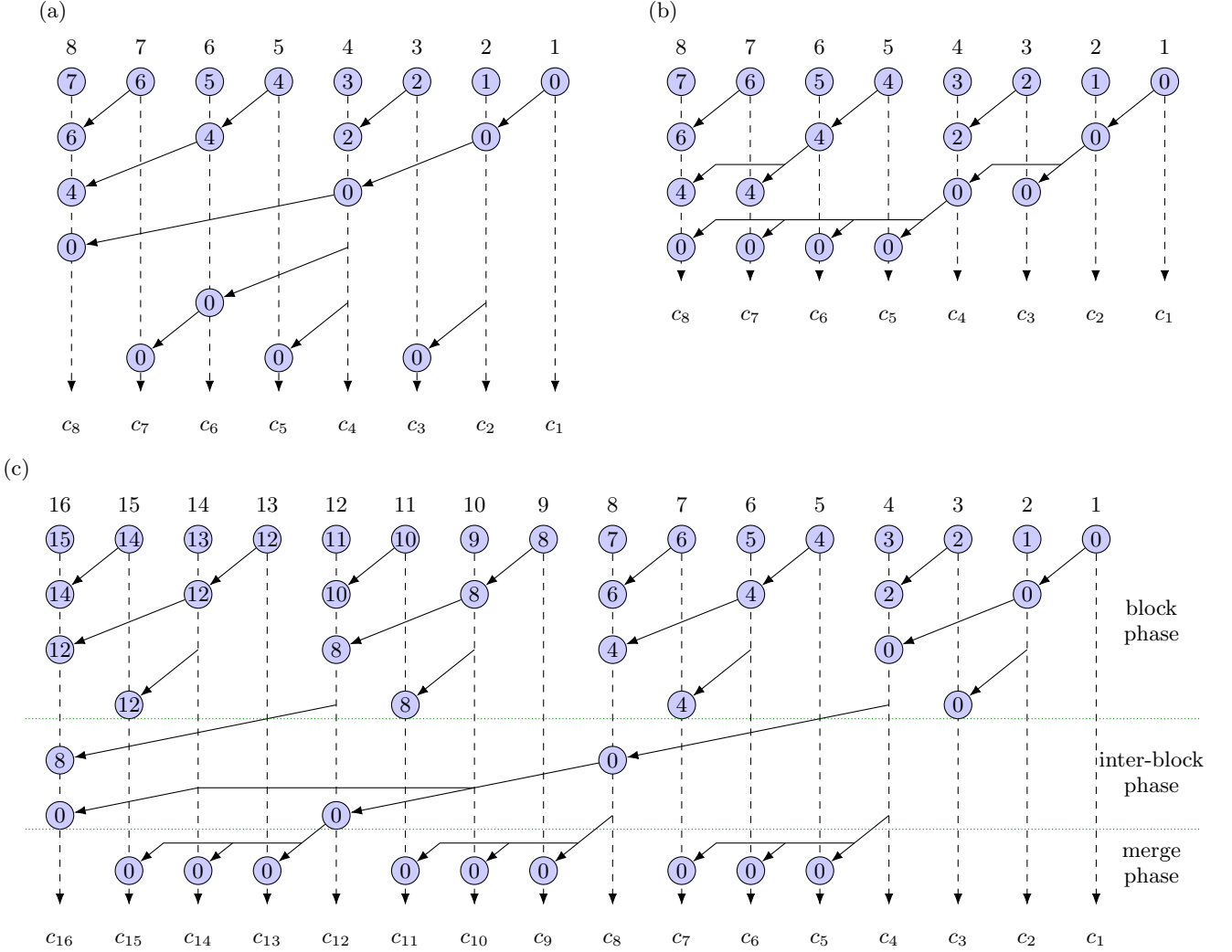


FIG. 5: Demonstration of carry bit computing by solving the prefix sum problem. Each column corresponds to a group of qubits that store the values of p and g , while each row represents a layer of Toffoli gates. If the j -th column is labeled i , it indicates that the values of $p[i, j]$ and $g[i, j]$ are stored in the qubits. Since $p[i, k]$ and $g[i, k]$ can be derived from $p[i, j]$, $g[i, j]$ together with $p[j, k]$, $g[j, k]$, the label of the k -th column can be updated from j to i whenever the j -th column is already labeled i . Proceeding in this way, the process eventually labels every column with 0, meaning that $g[0, i]$ has been obtained for all i . These values correspond exactly to the carry bits. (a) Method based on the Brent-Kung tree [29]. (b) Method based on the Sklansky tree [30]. (c) Our method combining both approaches.

B. In-place Quantum Adder

Suppose we have successfully computed the carry bits c , i.e., $|x\rangle|y\rangle|0\rangle \mapsto |x\rangle|y\rangle|c\rangle$. To obtain an in-place adder $|x\rangle|y\rangle|0\rangle \mapsto |x\rangle|s\rangle|0\rangle$ with $s = x + y$, we first apply CNOT gates to compute $|x\rangle|s\rangle|c\rangle$ using the relation $s_i = x_i \oplus y_i \oplus c_i$. The remaining task is to uncompute the carry register $|c\rangle$, which can be accomplished by a standard trick. For the n -bit sum $s = x + y$, let s' denote its bitwise complement, i.e., $s' = 2^n - x - y - 1 = x \oplus y \oplus c \oplus (-1)$, where we use \oplus denotes bitwise XOR for simplicity. Noting that $x + s' = x + (2^n - x - y - 1) = 2^n - y - 1 = y'$, and denoting the carry string generated by x and s' as c' , we find

$$\begin{aligned}
 x \oplus s' \oplus c' &= y', \\
 x \oplus (x \oplus y \oplus c \oplus (-1)) \oplus c' &= y \oplus (-1), \\
 c' &= c.
 \end{aligned} \tag{8}$$

Therefore, the carry-bit string generated by (x, s') is identical to that generated by (x, y) . Consequently, after computing s and c , we may negate s to obtain s' , and then recompute the carry bits in reverse to erase c . The complete procedure is summarized in Algorithm 3.

For clarity, we denote the Toffoli depth of the carry-bit computation as d_t , the Toffoli count as n_t , the CNOT depth as d_c , the CNOT count as n_c , and the ancilla overhead as s_a . In our in-place adder, the procedure requires $2n$ input qubits, one output qubit for the leading carry bit (which may be omitted), and $s_a + n$ ancillas. The overall Toffoli depth is $2d_t + 2$, with Toffoli count $2n_t + 2n - 1$, and the CNOT depth is $2d_c + 4$, with CNOT count $2n_c + 4n - 5$. When instantiated with our carry-bit computation scheme, the leading terms of these costs become

$$\begin{aligned}
\text{Toffoli depth} &= 2 \log n + 2 \log \log n + O(1), \\
\text{Toffoli number} &= 14n + O(1), \\
\text{CNOT depth} &= 2 \log n + 2 \log \log n + O(1), \\
\text{CNOT number} &= 17n + O(1), \\
\text{Ancilla} &= 4n + O(1).
\end{aligned} \tag{9}$$

Moreover, integer subtraction $|x\rangle|y\rangle \mapsto |x\rangle|x-y\rangle$ can be reduced to integer addition combined with two layers of bit flips. Specifically, we can first apply Pauli- X gates to flip all bits of x , obtaining $|\bar{x}\rangle = X^{\otimes n}|x\rangle = |2^n - x - 1\rangle$, perform the integer addition, and then flip $|\bar{x}\rangle$ and the outcome bits back. Since X gates are not counted in our resource analysis, integer subtraction is equivalent to integer addition in the following discussion.

Algorithm 3: quantum algorithm for in-place adder.

Function InPlaceAdder ($x; y; c[n]; c[1, \dots, n-1], a$):

Input : n -qubit number x ; n -qubit number y ; n -qubit s , initialized to 0; ancilla a (size depends on **ComputeCarry**), initialized to 0.

Output: $x, c[1, \dots, n-1], a$ remain the same; y holds sum bits; $c[n]$ holds the leading carry bit.

```

1   $c[i+1] \oplus= x[i]y[i]$  for  $i \leftarrow 0, \dots, n-1$ ;           // set  $c[i+1] = g[i, i+1]$ 
2   $y[i] \oplus= x[i]$  for  $i \leftarrow 0, \dots, n-1$ ;           // set  $y[i] = p[i, i+1]$  for  $i \geq 1$ ;  $y[0] = s_0$ 
3  ComputeCarry( $y; c; a$ );                               // set  $c[i] = c_i$  for  $i \geq 1$ 
4   $y[i] \oplus= c[i]$  for  $i \leftarrow 1, \dots, n-1$ ;         // set  $y[i] = s_i$ 
5   $y[i] = -y[i]$  for  $i \leftarrow 0, \dots, n-2$ ;         // negate  $y$  to get  $s'$ 
6   $y[i] \oplus= x[i]$  for  $i \leftarrow 1, \dots, n-2$ ;         // set  $y[i] = p'[i, i+1]$  for  $s'$  and  $x$ 
7  ComputeCarry-1( $y; c; a$ );                             // set  $c[i+1] = g'[i, i+1] = x_i \cdot s'_i$  for  $i \leq n-1$ 
8   $y[i] \oplus= x[i]$  for  $i \leftarrow 1, \dots, n-2$ ;         // recover  $y$  to  $s'$ 
9   $c[i+1] \oplus= x[i]y[i]$  for  $i \leftarrow 0, \dots, n-2$ ;   // recover  $c$  to 0 for  $i \leq n-1$ 
10  $y[i] = -y[i]$  for  $i \leftarrow 0, \dots, n-2$ ;         // recover  $y$  to  $s$ 

```

IV. CIRCUIT ANALYSIS

In this section, we present the quantum circuits used in our analysis and evaluate their resource requirements. Since the full quantum circuit for Shor's algorithm is highly complex, we begin in Sec. IV A with the circuit for controlled point addition, which serves as a fundamental building block for the overall construction. The complete circuit, assembled from these building blocks, is described in Sec. IV B, and its resource requirements are analyzed in Sec. IV C.

A. Point Addition

In Shor's algorithm, one of the inputs to the elliptic-curve point addition is either P or Q , whose values are stored classically rather than in qubits. This allows us to embed the corresponding information directly into the unitary circuit, thereby eliminating the need for qubits to store P and Q and simplifying the overall design. Based on Algorithm 1, the quantum circuit for elliptic-curve point addition is shown in Fig. 6. The circuit involves two divisions, two (full) multiplications, one (full) squaring, and nine integer additions (all of them are modular), of which two additions can be performed in parallel. The implementation of integer addition is described in Sec. III. It also serves as the fundamental building block for multiplication and inversion, while division is implemented by combining

inversion with multiplication. The detailed constructions of multiplication and division are provided in Appendix C 2 and C 3.

Notably, since no in-place implementations of multiplication and division are currently available, we employ out-of-place versions, defined analogously to the out-of-place adder: $U|x\rangle|y\rangle|0\rangle = |x\rangle|y\rangle|x \cdot y\rangle$ and $U|x\rangle|y\rangle|0\rangle = |x\rangle|y\rangle|x/y\rangle$. Both multiplication and division require sequences of additions. To realize these operations within limited qubit space, we must adopt in-place addition as the basic building block, even though out-of-place addition typically achieves only about half the complexity. This necessity also motivates our exclusive focus on the in-place adder in Sec. III.

The presented circuit does not correctly handle the special case involving the identity element O . To avoid this issue, the quantum register is typically initialized to a state representing kG (for some integer k) rather than O [47]. Such initialization does not affect the correctness of the final result, as it only introduces a global phase shift after applying the quantum Fourier transform. Additionally, the circuit encounters difficulties when the condition $x_1 = x_2$ arises; however, the probability of this event is exponentially small [47] and therefore has a negligible effect on the fidelity of the algorithm's output.

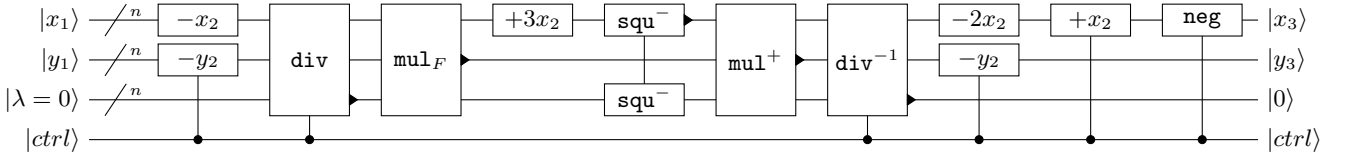


FIG. 6: Circuit for point addition. Here, $\pm a$ denotes the operation $|x\rangle \mapsto |(x \pm a) \bmod p\rangle$, **neg** denotes the operation $|x\rangle \mapsto |(-x) \bmod p\rangle$, **mul_F** denotes the operation $|x\rangle|y\rangle|z\rangle \mapsto |x\rangle|y\rangle|z \oplus (x \cdot y \bmod p)\rangle$ where \oplus is the bit-wise XOR, **mul⁺** denotes the operation $|x\rangle|y\rangle|z\rangle \mapsto |x\rangle|y\rangle|(x \cdot y + z) \bmod p\rangle$, **squ⁻** denotes the operation $|x\rangle|y\rangle \mapsto |(x - y^2) \bmod p\rangle|y\rangle$, and **div** denotes the operation $|x\rangle|y\rangle|0\rangle \mapsto |x\rangle|y\rangle|y/x \bmod p\rangle$. The \blacktriangleright in the circuit denotes the output qubit of an operation.

In terms of resource complexity, point addition requires Toffoli depth $56n \log n + 40n \frac{\log n}{\log \log n}$, Toffoli count $572n^2 + 140 \frac{n^2}{\log \log n}$, CNOT depth $48n \log n + 120n \frac{\log n}{\log \log n}$, and CNOT count $735n^2 + 40n^2 \frac{\log n}{\log \log n}$. The dominant contribution arises from division. Since division has been studied far less extensively than addition and exhibits substantially higher complexity, we expect it to provide the most promising avenue for further optimization.

The circuit for point addition requires $17n$ qubits in total, matching the cost of modular division, and has gate interaction distance 5. In each step of the procedure in Fig. 6, the qubits involved must maintain a fixed positional relationship. Our qubit layout is designed to satisfy this requirement wherever possible, while minor deviations can always be corrected with a constant number of SWAP operations, whose overhead is negligible compared to the overall algorithm.

B. Shor's Algorithm

If we directly apply the algorithm of Sec. II B, implementing the full point addition

$$\frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle|y\rangle|O\rangle \mapsto \frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle|y\rangle|xG + yQ\rangle \quad (10)$$

requires $2n$ controlled point additions, each conditioned on the corresponding bit of x or y . A detailed resource analysis shows that this construction has Toffoli depth $112n^2 \log n + o(n^2 \log n)$, Toffoli count $1144n^3 + o(n^3)$, and CNOT count $80n^3 \frac{\log n}{\log \log n} + 1490n^3 + o(n^3)$. The qubit cost is $17n$, the same as for a single point addition. As illustrated in Fig. 7, dynamic-circuit techniques can be employed to compress the $2n$ qubits of the registers $|x\rangle, |y\rangle$ used in the quantum Fourier transform into a single qubit, ensuring that no additional columns are introduced.

The windowed trick [26] can further reduce the overall resource cost. Intuitively, it groups multiple blocks of Fig. 7 into a single operation, thereby decreasing the number of point additions at the expense of additional pre-computing. In the naive approach, one requires $2n$ controlled point additions of the form $+G, +2G, +4G, \dots$ and $+Q, +2Q, +4Q, \dots$. In contrast, with a window size l , l control bits $|b = b_{l-1} \dots b_0\rangle$ are processed simultaneously. In the k -th window, the operation $+bP_k$ is applied, where $P_k = 2^{l(k-1)}P$ with $P \in \{G, Q\}$. The required value of bP_k is obtained from a quantum lookup table. This approach saves $l - 1$ point additions per window, at the cost of maintaining a table of 2^l pre-computed states. The resulting circuit is shown in Fig. 8.

The cost of quantum tables can be reduced by a factor of two using the signed trick. Define $b' = b - b_{l-1}2^{l-1}$, where b_{l-1} is the most significant bit of the window. If $b_{l-1} = 1$, we look up $b'P_k$; if $b_{l-1} = 0$, we instead look up $(2^{l-1} - b')P_k$ and apply a negation. Since $-P = (P_x, -P_y)$, this negation can be implemented by a simple **neg** operation on the y coordinate. The procedure effectively outputs $(b - 2^{l-1})P_k$, so the quantum table needs to store only 2^{l-1} entries rather than 2^l . This introduces only a global phase shift in each window after the QFT, which does not affect the final result.

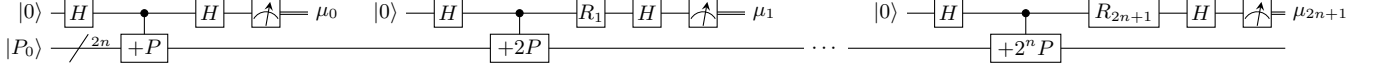


FIG. 7: Circuit for Shor’s algorithm. Each R_i is a z -rotational gate whose rotation angle is based on the previous measurement results $\mu_0, \mu_1, \dots, \mu_{i-1}$. The “+” in the blocks “ $+2^i P$ ” stand for point addition. P_0 is a random multiple of G to avoid adding on the identity element O , as discussed in [47].

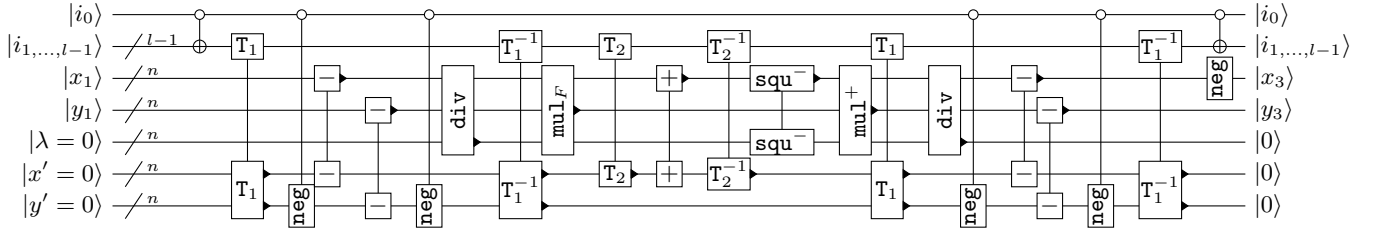


FIG. 8: The circuit for windowed point addition with window size l (the first window). Here, \pm denotes the operation $|x\rangle |y\rangle \mapsto |x\rangle |(y \pm x) \bmod p\rangle$, T_1 is the quantum table with input i and output $(iP)_x, (iP)_y$, where P is a point on the elliptic curve, T_2 is the quantum table with input i and output $3(iP)_x$, and the meanings of **neg**, **mul_F**, **mul⁺**, **squ⁻**, **div** are explained in the caption of Fig. 6.

Intuitively, the windowed trick reduces the number of point additions by a factor of l , but requires an additional $O(2^l)$ resources to construct the lookup table each time a point addition is performed. Since the Toffoli depth of a single point addition without windowing is $\Theta(n \log n)$, the optimal window size is $l = \log n + o(\log n)$ for sufficiently large n . The overall circuit still requires $17n$ qubits, as the extra l ancillas introduced by the window trick can be placed at the ends of existing columns. An illustration of the complete circuit is given in Fig. 9.

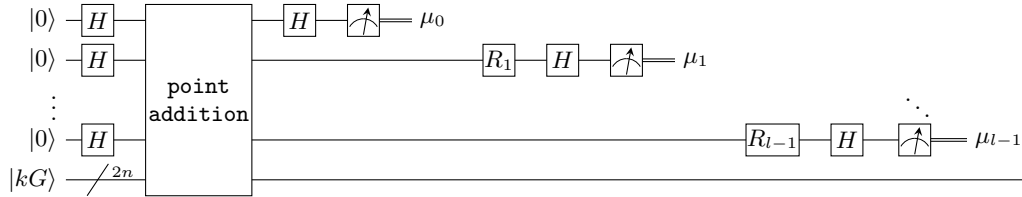


FIG. 9: The first cell for point addition, following Fig. 2 in [25]. The whole circuit consists of $\lceil \frac{2n}{l} \rceil$ cells. Here, R_k are rotation gates $\text{diag}(1, e^{i\theta_k})$, and $\theta_k = -\pi \sum_{j=0}^{k-1} 2^{k-j} \mu_j$ where $\mu_j \in \{0, 1\}$ is the measurement outcome.

C. Circuit Parameters

In this section, we summarize and explain the resource costs of our algorithm. Recall that the circuit consists of Pauli gates, H gates, S gates, CNOT gates, SWAP gates, and Toffoli gates (with Toffoli gates further decomposed into CNOT and H, T, T^\dagger gates). In our estimation, however, we count only CNOT and Toffoli gates. The reason for omitting Pauli, Hadamard, S , and SWAP gates is explained below.

Pauli gates can be eliminated entirely by a standard postponement trick. Since Y is proportional to XZ , it suffices to consider X and Z . When a Pauli gate P is encountered, we look ahead to the next operation. If the next gate is a Z -basis measurement, we simply measure first and apply the effect of P to the measurement result: X flips the outcome, while Z has no effect. If the next gate is another Pauli, the two can be combined. If it is a Clifford gate U , then $P' = UPU^\dagger$ is still a Pauli operator, and we may implement U first while postponing P . Finally, if the next gate is a non-Clifford, the only possibilities in our algorithm are T and T^\dagger . These commute with Z , and conjugation with X only changes T to T^\dagger or vice versa, so T and T^\dagger can also be applied first, leaving the Pauli gate postponed.

Hadamard and S gates, outside their role in Toffoli decompositions, occur only rarely in Shor’s algorithm. We therefore absorb their cost into that of the Toffoli gates.

SWAP gates are slightly different. Each SWAP can be decomposed into three CNOT gates, but we treat them separately to highlight the effect of the two-dimensional qubit layout. Specifically, our CNOT counts include only those gates required by the logical structure of the algorithm, while SWAP counts measure the additional gates needed to respect the interaction-distance constraints discussed in Sec. II C. Under this convention, the number of SWAPs turns out to be negligible, as shown in Appendix D.

With these conventions, our resource estimates include qubit count, CNOT depth, CNOT count, Toffoli depth, and Toffoli count. Exact costs for inputs of 25, 192, 256, 384, and 521 bits, together with the leading-order terms for general n , are summarized in Table II. A brief explanation of these items is given below, which is the same as that in Sec. I.

CNOT depth and count measure only the CNOT gates that arise directly from the algorithm itself, including those in addition, in the construction of quantum tables, and in the translation steps of multiplication and division. Detailed derivations are presented in Appendix C.

Toffoli depth and count are the most important parameters, since under error-correcting codes such as the surface code, Toffoli gates dominate both time and fidelity costs. Our adjustable parameters, namely the window sizes, are chosen specifically to minimize Toffoli depth. Almost all Toffoli gates in the algorithm are long-range gates implemented by dynamic circuits.

V. DISCUSSION

Although quantum algorithms for integer factoring have received extensive attention, far fewer works have systematically addressed Shor’s elliptic curve algorithm, despite its comparable importance in modern cryptography. Our study fills this gap by presenting a complete implementation and resource analysis of Shor’s elliptic curve algorithm tailored to two-dimensional nearest-neighbor architectures. The key enabling technique is the use of dynamic circuits, which allow long-range Toffoli gates and unbounded GHZ states to be realized with constant overhead. These primitives provide the essential capabilities for long-distance qubit interaction and parallel execution of controlled operations. By incorporating them into the design of modular arithmetic, we demonstrate that the elliptic curve discrete logarithm problem can be realistically compiled for hardware-constrained architectures with an acceptable overhead, and give a detailed resource analysis on qubit number, CNOT depth and counts, and Toffoli depth and counts. Our results therefore establish a concrete baseline for the future experimental realization of quantum attacks on elliptic curve cryptography.

Beyond the application of the elliptic curve discrete logarithm problem, our work makes contributions of broader relevance. A central technical advance is our improved carry-lookahead adder, which achieves best-known Toffoli depth while requiring only linear ancilla overhead. Since addition is a ubiquitous subroutine across quantum algorithms—including factoring, lattice problems, and quantum simulation—this design has potential applications well beyond elliptic curves.

At the same time, our analysis reveals that the dominant resource cost of Shor’s elliptic curve algorithm arises from modular division. As this operation is far less studied than addition and is substantially more expensive, improving quantum modular division directly promises to lower the overall cost of Shor’s elliptic curve algorithm and represents a natural target for further optimization.

It is also instructive to compare our findings with recent resource estimates for factoring-based cryptanalysis [24]. Classically, the security of 256-bit elliptic curve cryptography is considered comparable to that of 3072-bit RSA. However, our analysis shows that the quantum resources required to break these problems differ substantially. Solving the 256-bit elliptic curve cryptography requires about 2.25 times more qubits than solving the 3072-bit RSA problem, but only about 1/13 as many Toffoli gates. This contrast suggests that, under realistic quantum architectures, elliptic-curve-based systems may be more vulnerable to large-scale quantum attacks than RSA, despite their stronger classical security guarantees.

Our results also highlight several avenues for future improvement. While our construction is adapted to a two-dimensional topology, this constraint inevitably imposes additional overhead. In particular, our layout arranges qubits

in a long, narrow configuration, which increases the reliance on dynamic circuits to mediate long-range interactions. For example, SWAP operations used to implement long-range Toffoli gates (see Sec. IID) dominate the SWAP cost of the entire algorithm. A more flexible qubit topology, featuring enhanced connectivity beyond nearest neighbors or a square rather than rectangular arrangement of qubits, can mitigate this overhead by reducing the frequency of dynamic-circuit primitives and lowering the associated resource requirements.

Finally, we note that our analysis has been carried out at the logical gate level, without considering the detailed implementation of quantum error correction (QEC). Since Toffoli gates dominate both runtime and error budgets under leading error-correcting codes, a more detailed QEC-based analysis would provide valuable insights into fault-tolerant cost and overhead. Such work would be an important next step toward connecting algorithmic resource estimates with the concrete capabilities of near-future hardware.

ACKNOWLEDGMENTS

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Appendix B: Previous Works of Carry Bit Computing

In this section, we introduce two previous works of carry bit computing and their advantages and disadvantages, which serves as building blocks of our work. For convenience, we define the weight of n

$$w(n) = n - \sum_{i=1}^{\infty} \left\lfloor \frac{n}{2^i} \right\rfloor \quad (\text{B1})$$

as the number of ones in the binary representation of n . We have the following lemma

Lemma 1. *For any integer $n \geq 1$, we have*

$$\sum_{i=0}^{n-1} w(i) \leq \frac{1}{2} n \log n, \quad (\text{B2})$$

whose proof is given in Appendix B3.

1. Algorithm based on Brent-Kung tree

The first algorithm for quantum carry-lookahead adder is given in [29]. This method uses the Brent-Kung prefix tree, as shown in Fig. 5a. The detail of the corresponding classical algorithm is described in Algorithm 4. We need $p[i-1, i]$ and $g[i-1, i]$ as the input, both of which can be computed directly using the input. We separate each round of the carry-bit computing into four stages, as shown in Algorithm 4. In round t of stage P_1 , we let $P_t[m] = p[2^t m, 2^t(m+1)]$. In round t of stage G_1 , we let $G[2^t m + 2^t] = g[2^t m, 2^t(m+1)]$. In round t of stage P_2 , we let $P'_t[m] = p[0, 2^t m + 2^{t-1}]$. In round t of G_2 , we let $G[2^t m + 2^{t-1}] = g[0, 2^t m + 2^{t-1}]$. P_1, P_2 use logical AND gate with output initialized in $|0\rangle$, which requires one ancilla. G_1, G_2 use logical AND gate with nonzero output which requires two ancillas. Moreover, when we need to recover the carry bit, there are two stages in each round, denoted by P_1^{-1} and P_2^{-1} . Each round of P_1^{-1} and P_2^{-1} use only uncomputation AND gate and therefore need no T gate.

There are two methods to parallelize this algorithm. In the first one, we parallelize the t -th round of stage P_1 with the t -th round of stage G_1 . It requires that P_{t-1} serves as the control bit for stage P_1 and stage G_1 simultaneously. Thus, we need a CNOT gate to copy it, followed by another CNOT gate to recover it afterwards, as shown in Fig. 12. In this case, we need two ancillary qubits for parallelization of a Toffoli in stage P_1 and a Toffoli in stage G_1 , one of which for copy, the other one for a general Toffoli gate implementation. Since there are $\lfloor n/2^t \rfloor$ pairs of such Toffoli gates implementing simultaneously in round t , we need at most $\frac{n}{2} \cdot 2 = n$ ancillas. The parallelization of stage P_2 and G_2 is exactly the same. In total, we need n input qubits, $2n - w(n) - \lfloor \log n \rfloor - 1$ output qubits, n input and output qubits, and n ancillary qubits. The Toffoli/CNOT depth/count of this method is

$$\begin{aligned} \text{Toffoli depth} &= \lfloor \log n \rfloor + \left\lceil \log \frac{2n}{3} \right\rceil, \\ \text{Toffoli count} &= 4n - 2w(n) - 2\lfloor \log n \rfloor - 2, \\ \text{CNOT depth} &= \lfloor \log n \rfloor + \left\lceil \log \frac{2n}{3} \right\rceil + 2, \\ \text{CNOT count} &= 4n - 2w(n) - 2\lfloor \log n \rfloor - 2. \end{aligned} \quad (\text{B3})$$

In the second method, we parallelize the t -th round of stage P_1 and the $(t-1)$ -th round of stage G_1 . In this case, there is no qubit serving as the control bits for both stage, and we no longer need the CNOT gates for copying and recovering. Therefore, the maximum number of ancillas we need is $\frac{n}{2}$. The Toffoli depth and number of this method is

$$\begin{aligned} \text{Toffoli depth} &= \lfloor \log n \rfloor + \left\lceil \log \frac{2n}{3} \right\rceil + 2, \\ \text{Toffoli number} &= 4n - 2w(n) - 2\lfloor \log n \rfloor - 2, \end{aligned} \quad (\text{B4})$$

and it need no CNOT gates.

Comparing these two methods, we can see that the first method reduces the Toffoli depth by two at the cost of $0.5n$ more ancillas and $2 \log n$ CNOT depth. The extra ancillas do not matter a lot, since the space overhead of this

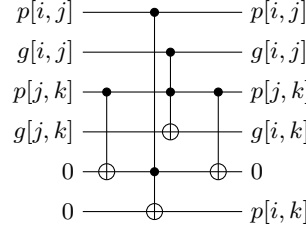


FIG. 12: The first method to parallelize the carry computing procedure. Note that the second CNOT can be parallelized with the first one in the next round. The CNOT depth in the carry computing part is only larger than the Toffoli depth by 1.

part is not the bottleneck of our final algorithm, as we will explain later. Whether it is worthy to replace two Toffoli depth with $2 \log n$ CNOT depth, however, depends on the specific application. Since our Toffoli gate implementation have a CNOT depth of at least 6, as shown in Fig. 10, it is always better to use the first method when $n \leq 64$, if we only consider the depth. Furthermore, in many fault-tolerant quantum computing schemes, the time overhead of T gates could be much larger than that for CNOT gates, making the CNOT depth less important than T -depth as a measure of algorithm performance. In this case, the strict superiority of the first method can be achieved for the qubit number smaller than a threshold t , which can be much larger than 64. In this paper, we use the first method for the sake of simplicity.

We should remark that the carry-bit computing introduced here is slightly more expensive than the initial one in [29]. The reason is that some of the propagation state computation (stage P_2 and the final round in stage P_1) is unnecessary if we only need the carry bits $g[0, i]$. However, the propagation bits $p[0, i]$ are also useful in our algorithm, making us retain this part. Such a difference, after all, will not affect the Toffoli depth.

Algorithm 4: quantum algorithm for computing carry bits based on Brent-Kung tree.

```

Function ComputeCarryDraperPGCompute( $P_0; G; P; a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $n$ -qubit  $G$  storing  $g[i-1, i]$ ;  $(2n - w(n) - \lfloor \log n \rfloor - 1)$ -qubit  $P$ , initialized to
           0;  $2n$ -qubit ancilla  $a$ , initialized to 0.
  Output:  $P_0, a$  remains the same;  $G$  holds carry bits  $c_i = g[0, i]$ ;  $P$  holds propagation states, including  $p[0, i]$ .
1  for  $t \leftarrow 1, \dots, \lfloor \log n \rfloor$  do
2     $P_t[m] = P_{t-1}[2m] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 0, \dots, \lfloor n/2^t \rfloor$ ; // stage  $P_1$ 
3     $G[2^t m + 2^t] \oplus = G[2^t m + 2^{t-1}] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 0, \dots, \lfloor n/2^t \rfloor$ ; // stage  $G_1$ 
4  for  $t \leftarrow \lfloor \log \frac{2n}{3} \rfloor, \dots, 1$  do
5     $P'_t[m] = P_t[0] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 1, \dots, \lfloor (n - 2^{t-1})/2^t \rfloor$ ; // stage  $P_2$ 
6     $G[2^t m + 2^{t-1}] \oplus = G[2^t m] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 1, \dots, \lfloor (n - 2^{t-1})/2^t \rfloor$ ; // stage  $G_2$ 

Function ComputeCarryDraperPUncompute( $P_0; P; a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $(2n - w(n) - \lfloor \log n \rfloor - 1)$ -qubit  $P$  storing propagation states;  $n$ -bit ancilla,
           initialized to 0.
  Output:  $P_0$  remains the same;  $P$  recovered to 0.
7  for  $t \leftarrow 1, \dots, \lfloor \log \frac{2n}{3} \rfloor$  do
8     $P'_t[m] \oplus = P_t[0] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 1, \dots, \lfloor (n - 2^{t-1})/2^t \rfloor$ ; // stage  $P_2^{-1}$ 
9  for  $t \leftarrow \lfloor \log n \rfloor, \dots, 1$  do
10    $P_t[m] \oplus = P_{t-1}[2m] \cdot P_{t-1}[2m+1]$  for  $m \leftarrow 0, \dots, \lfloor n/2^t \rfloor$ ; // stage  $P_1^{-1}$ 

Function ComputeCarryDraper( $P_0; G; P; a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $n$ -qubit  $G$  storing  $g[i-1, i]$ ;  $(2n - w(n) - \lfloor \log n \rfloor - 1)$ -qubit ancilla  $P$  and
            $2n$ -qubit ancilla  $a$ , initialized to 0.
  Output:  $P_0, P, a$  remains the same;  $G$  holds carry bits  $c_i = g[0, i]$ .
11 ComputeCarryDraperPGCompute( $P_0, G, P, a$ );
12 ComputeCarryDraperPUncompute( $P_0, P$ );

```

2. Algorithm based on Sklansky tree

A new method for computing the carry bits based on the Sklansky prefix tree is proposed in [30], as shown in Fig. 5b. This method halves the Toffoli depth of the previous method, at the cost of linear fan-out and increasing the ancilla space overhead to $O(n \log n)$. The algorithm is shown in Algorithm 5. We separate each round of the carry-bit computing into two stages. In the t -th round of stage P , we set $P_k[l, m] = p[2^k \cdot l, 2^k \cdot l + m]$, and in the t -th round of stage G , we set $G[2^k \cdot l + m] = g[2^k \cdot l, 2^k \cdot l + m]$. Similar to the previous method, stage P and G use logical AND gates, and stage P^{-1} uses uncomputation gates.

We still have two parallelization methods. The first method parallelizes round t of stage P and round t of stage G , which needs CNOT gates. There are $\frac{n}{2}$ Toffoli gates in stage P and stage G implemented simultaneously, implying that the ancillas needed is $\frac{n}{2} \cdot (1 + 1) = n$. In total, we need n input qubits, $\frac{n}{2} \log n$ output qubits, n input and output qubits, and n ancillas. The Toffoli/CNOT cost of this method is

$$\begin{aligned} \text{Toffoli depth} &= \lceil \log n \rceil, \\ \text{Toffoli number} &= 2 \sum_{i=0}^{n-1} w(i) \leq n \log n, \\ \text{CNOT depth} &= \lceil \log n \rceil + 1, \\ \text{CNOT number} &= 2 \sum_{i=0}^{n-1} w(i) \leq n \log n, \end{aligned} \tag{B5}$$

where the inequality is from Lemma 1.

The second method parallelizes round t of stage P and round $t - 1$ of stage G , with resource cost

$$\begin{aligned} \text{Toffoli depth} &= \lceil \log n \rceil + 1, \\ \text{Toffoli number} &= 2 \sum_{i=0}^{n-1} w(i) \leq n \log n, \end{aligned} \tag{B6}$$

with no CNOT gates. The ancillas needed in this method is $\frac{n}{2}$. Again, we choose the first method in this paper.

3. Proof of Lemma 1

For simplicity, we define $S_n = \sum_{i=0}^{n-1} w(i)$, and let $S_0 = 0$. We have two observations of S_n :

Observation 1. *If $n = 2^k$ for some non-negative integer k , $S_n = \frac{1}{2}n \log n$.*

Observation 2. *For any integer $n \geq 1$, let $k = \lfloor \log n \rfloor$, then*

$$\begin{aligned} S_n &= S_{2^k} + (n - 2^k) + S_{n-2^k} \\ &= n - 2^k + \frac{1}{2}k2^k + S_{n-2^k}, \end{aligned} \tag{B7}$$

where the second equality is from Observation 1.

Now, we begin our proof by induction on n . The base cases $n = 1, 2$ are trivial. Suppose the lemma holds for all integers smaller than n . If $\log n \in \mathbb{Z}$, the inequality holds by Observation 1. Thus, we only need to consider the cases $\log n \notin \mathbb{Z}$ from now on. Let $k = \lfloor \log n \rfloor$. By Observation 2, we have

$$S_n = n - 2^k + \frac{1}{2}k2^k + S_{n-2^k} \leq n - 2^k + \frac{1}{2}k2^k + \frac{1}{2}(n - 2^k) \log(n - 2^k). \tag{B8}$$

Let $f(x) = n - x + \frac{1}{2}x \log x + \frac{1}{2}(n - x) \log(n - x)$. We only need to prove $f(2^k) \leq \frac{1}{2}n \log n$. Note that $\frac{n}{2} < 2^k < n$, we can generalize the statement and try to prove that $f(x) \leq \frac{1}{2}n \log n$ for all $x \in (\frac{n}{2}, n)$. Taking the derivative of $f(x)$, we have

$$f'(x) = \frac{1}{2} \log \frac{x}{n-x} - 1, \tag{B9}$$

$$f''(x) = \frac{1}{2} \left(\frac{1}{x} + \frac{1}{n-x} \right) > 0. \tag{B10}$$

Algorithm 5: quantum algorithm for computing carry bits based on Sklansky tree.

```

Function ComputeCarryWangPGCompute( $P_0; G; P; a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $n$ -qubit  $G$  storing  $g[i-1, i]$ ;  $\frac{n}{2} \log n$ -qubit  $P$ , initialized to 0;  $2n$ -qubit ancilla
     $a$ , initialized to 0.
  Output:  $P_0, a$  remains the same;  $G$  holds carry bits  $c_i = g[0, i]$ ;  $P$  holds propagation states, including  $p[0, i]$ .
1  for  $k \leftarrow 1, \dots, \lceil \log n \rceil - 1$ ; // stage  $P$ 
2  do
3    for  $l \leftarrow 1, \dots, \lceil n/2^k \rceil$  do
4    [  $P_k[l, m] = P_{k-1}[2l, 2^{k-1}] \cdot P_{k-1}[2l+1, m-2^{k-1}]$  for  $m \leftarrow 2^{k-1}+1, \dots, \min\{2^k, n-2^{k-1}(2l+1)\}$ 
5  for  $k \leftarrow 1, \dots, \lceil \log n \rceil$ ; // stage  $G$ 
6  do
7    for  $l \leftarrow 0, \dots, \lceil n/2^k \rceil$  do
8    [  $G[2^k \cdot l + m] \oplus = G[2^{k-1}(2l+1)] \cdot P_{k-1}[2l+1, m-2^{k-1}]$  for  $m \leftarrow 2^{k-1}+1, \dots, \min\{2^k, n-2^{k-1}(2l+1)\}$ 

Function ComputeCarryWangPUncompute( $P_0; P$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $\frac{n}{2} \log n$ -qubit  $P$  storing propagation states.
  Output:  $P_0$  remains the same;  $P$  recovered to 0.
9  for  $k \leftarrow \lceil \log n \rceil - 1, \dots, 1$ ; // stage  $P^{-1}$ 
10 do
11 [ for  $l \leftarrow \lceil n/2^k \rceil, \dots, 1$  do
12 [  $P_k[l, m] \oplus = P_{k-1}[2l, 2^{k-1}] \cdot P_{k-1}[2l+1, m-2^{k-1}]$  for  $m \leftarrow 2^{k-1}+1, \dots, \min\{2^k, n-2^{k-1}(2l+1)\}$ 

Function ComputeCarryWang( $P_0; G; P; a$ ):
  Input :  $n$ -qubit  $P_0$  storing  $p[i-1, i]$ ;  $n$ -qubit  $G$  storing  $g[i-1, i]$ ;  $\frac{n}{2} \log n$ -qubit ancilla  $P$  and  $2n$ -qubit ancilla  $a$ ,
    initialized to 0.
  Output:  $P_0, P, a$  remains the same;  $G$  holds carry bits  $c_i = g[0, i]$ .
13 ComputeCarryWangPGCompute( $P_0, G, P, a$ );
14 ComputeCarryWangPUncompute( $P_0, P$ );

```

Furthermore, we have $f'(\frac{n}{2}) = -1 < 0$ and $\lim_{x \rightarrow n} f'(x) = +\infty > 0$. We can conclude that $f(x)$ first decreases and then increases in the interval $(\frac{n}{2}, n)$, which implies that $f(x) \leq \max\{f(\frac{n}{2}), \lim_{x \rightarrow n} f(x)\}$. Given

$$f\left(\frac{n}{2}\right) = \frac{n}{2} + \frac{n}{4} \log \frac{n}{2} + \frac{n}{4} \log \frac{n}{2} = \frac{1}{2}n \log n, \quad (\text{B11})$$

$$\lim_{x \rightarrow n} f(x) = 0 + \frac{1}{2}n \log n + 0 = \frac{1}{2}n \log n, \quad (\text{B12})$$

we have $f(x) \leq \frac{1}{2}n \log n$ for $x \in (\frac{n}{2}, n)$, which completes our proof.

Appendix C: Circuit Construction

In this section, we introduce the circuit for the components of point addition, including modular addition, modular multiplication and modular division, followed by a detailed analysis of resource consumption, including circuit depth, width and gate number. Recall that modular addition implements $|x\rangle|y\rangle \mapsto |x\rangle|(y+x) \bmod p\rangle$, modular multiplication implements $|x\rangle|y\rangle|z\rangle \mapsto |x\rangle|y\rangle|(z \oplus x \cdot y) \bmod p\rangle$, and modular division implements $|x\rangle|y\rangle|z\rangle \mapsto |x\rangle|y\rangle|(z \oplus \frac{y}{x}) \bmod p\rangle$. We will only discuss Toffoli depth, Toffoli number, CNOT depth, and CNOT number as explained in Sec. IV C, and will mainly focus on their leading terms. Specifically, as an example, if we say “the Toffoli depth is $4n \log n$ ” for simplicity, we actually mean “the Toffoli depth is $4n \log n + o(n \log n)$ ”. For equations, we will use “=” for precise numbers, and “ \simeq ” for asymptotic equivalence up to leading terms. That is, $x \simeq f(n)$ means $x = f(n) + o(f(n))$. Since Toffoli gates are the most time-consuming part in our circuit, our main optimization goal is to make Toffoli depth as small as possible.

For simplicity, this section will only include the main operations, and will only include the result of the resource cost of these operations. Detailed computation of the resource cost can be found in Appendix D. Other circuit constructions can be found in Appendix E.

1. Modular Addition

Recall that we have discussed integer addition in detail in Sec. III. The key idea of implementing modular addition with integer addition is to use a sign qubit to decide whether $x + y$ is greater than p or not [25]. To be specific, one can apply the integer addition $|x\rangle|y\rangle \mapsto |x\rangle|x+y\rangle$, followed by a constant addition $-p$ controlled by whether $x + y - p$ is positive or not. By utilizing the leading carry bit of $x + y - p$ as the controlled bit, one realize the former idea with a single controlled constant addition [49]. Moreover, to recover the sign qubit, a comparator that realize $|x\rangle|y\rangle|b\rangle \mapsto |x\rangle|y\rangle|b \oplus c(x, y)\rangle$ is applied to the final state, where $c(x, y) = 0$ if $x > y$ and $c(x, y) = 1$ otherwise. The former procedure is shown by the circuit in Fig. 13, and detailed discussions for the constructions of constant addition and comparator are given in Appendices E3b and E3c.

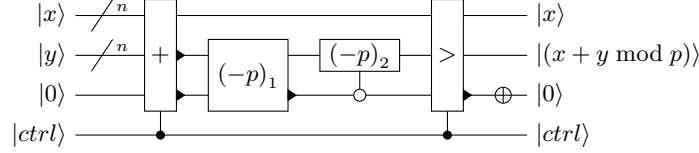


FIG. 13: Circuit for controlled modular addition [26]. Here, “+” denotes controlled integer addition, “ $-p$ ” denotes controlled constant subtraction of p where “ $(-p)_1$ ” and “ $(-p)_2$ ” are the two parts of one controlled constant subtraction, as explained in Appendix E3b, “ $>$ ” denotes controlled comparator, and \oplus means a Pauli X operation. Note that the first “+” has one more qubit output, which is the highest carry bit, since $x + y$ can be an $(n + 1)$ -bit number.

In Shor’s algorithm, the required operation is a controlled modular addition, indicating that all gates in the addition circuit must be conditioned on a control qubit, denoted as $ctrl$, as illustrated in Fig. 13 [25]. It is worth noting that, except for the integer addition and comparator components, the remaining operations, labeled “ $(-p)_1$ ”, “ $(-p)_2$ ”, and “ \oplus ”, mutually cancel when the circuit is executed in sequence. Consequently, the control need only be applied to the integer addition and comparator subroutines. The detailed implementations of the controlled integer adder and controlled comparator are provided in Appendices E3b and E3c.

We now analyze the qubit layout for modular addition. As discussed in Sec. III, the integer addition requires $4n$ ancillary qubits, corresponding to four columns in our layout. Beyond these, no additional column is needed to store the constant p , since its value is embedded directly through the simplification of constant addition. Likewise, no separate column is required for the control qubit, as it can be conveniently prepared from the ancillas of the addition circuit whenever needed. The resulting layout is illustrated in Fig. 14. The maximum gate interaction distance is 2, occurring between the $|y\rangle$ register and the ancillary qubits p_1 and g . Overall, the modular addition circuit requires a Toffoli depth of $(5 \log n + 4 \log \log n)$, a Toffoli count of $33n$, a CNOT depth of $(5 \log n + 4 \log \log n)$, and a CNOT count of $42n$. A detailed breakdown of these resource estimates is provided in Appendix D.

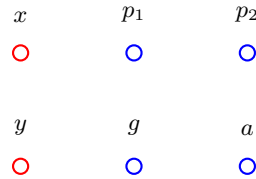


FIG. 14: Qubits layout for modular addition. Each point stands for a column of n qubits. Red points x, y are data qubits, and blue points p_1, p_2, g , and a are ancillary qubits.

2. Modular Multiplication

The modular multiplication implements $|x\rangle|y\rangle|z\rangle \mapsto |x\rangle|y\rangle|z \oplus (x \cdot y \bmod p)\rangle$. To make the multiplication more efficient, we choose the Montgomery representation [31] rather than the normal binary representation. In the Montgomery representation, an integer x is expressed as $x' = x2^n \bmod p$, where $n = \lceil \log p \rceil$. Therefore, any integer in this representation is intrinsically mod p . Note that the addition in Montgomery representation is the consistent to that in standard representation since $x' + y' = (x + y)2^n \bmod p = (x + y)'$. Moreover, to compute $x \cdot y$, we first compute $x' \cdot y' = x \cdot y \cdot 2^{2n} \bmod p$, then perform a 2^n reduction to get $(x \cdot y)' = x \cdot y \cdot 2^n \bmod p$.

To achieve modular multiplication in the Montgomery representation, we first initialize one column of n qubits to $|0^n\rangle$ as the output qubits. Denote the binary representation of x as $x = x_{n-1} \dots x_1 x_0$. In the i -th step, we add y to the result conditioned on whether x_i is 1 or not, and perform a 2-reduction. A 2-reduction $|x\rangle \mapsto |x/2 \bmod p\rangle$ is achieved through a controlled $+p$ conditioned on whether x is odd or even, followed by a right shift, which is similar to what we do in our modular addition. This method computes

$$((x_0 y/2 + x_1 y)/2 + \dots + x_{n-1} y)/2 \bmod p = (x_0 + x_1 2^1 + \dots + x_{n-1} 2^{n-1}) \cdot y/2^n \bmod p = (x \cdot y)/2^n \bmod p, \quad (\text{C1})$$

which is the Montgomery representation of $x \cdot y$.

In total, this method requires n controlled additions, n controlled constant additions, and n one-bit right shifts. Right shifts are achieved with SWAP gates and need no Toffoli gate. Since each addition costs $4 \log n$ Toffoli depth, this method costs $8n \log n$ Toffoli depth. The circuit of this method of modular multiplication is shown in Fig. 15.

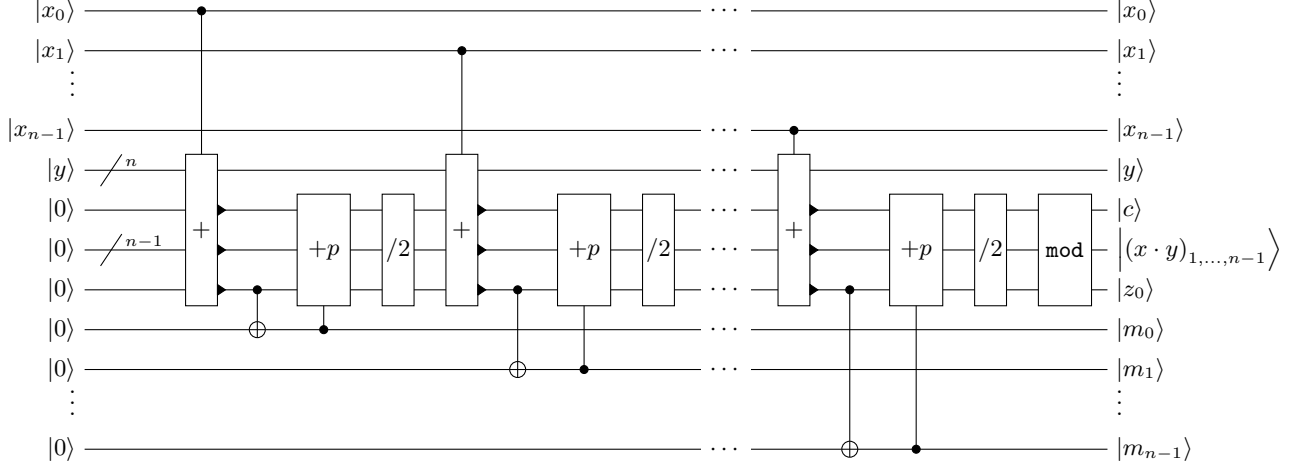


FIG. 15: Quantum circuit for modular multiplication without the windowed trick. The “+” (modular addition) operation performs the transformation $|y\rangle |0\rangle |z_{n-1} \dots z_1\rangle |z_0\rangle \mapsto |y\rangle |c'\rangle |z'_{n-1} \dots z'_1\rangle |z'_0\rangle$, where c' denotes the highest carry bit and $z' = (z + y) \bmod p$. Here, z_0 and z'_0 are the least significant bits of z and z' , respectively. The highest carry bit c' can be regarded as z_n , effectively extending z to an $(n + 1)$ -bit string. The “+ p ” block represents a (controlled) constant integer addition, as discussed in Appendix E 3 b. The “/2” block denotes a (controlled) 1-bit right shifting operation, as discussed in Appendix E 4 b. mod corresponds to the modular reduction, as discussed in Appendix E 3 d.

The windowed trick [50] can be employed to further reduce the computational cost. In the previous procedure, the value of y is added conditionally based on a single bit x_i during the i -th step. Instead, we can consider a k -bit segment of x , and use it to control the y -addition to the output register in a single step. More precisely, the n -bit string x can be partitioned into disjoint k -bit blocks $x_{(\lfloor \frac{n}{k} \rfloor)}, x_{(\lfloor \frac{n}{k} \rfloor - 1)}, \dots, x_{(0)}$, where

$$x_{(0)} = x_{k-1} \dots x_0; \quad x_{(1)} = x_{2k-1} \dots x_k; \quad \dots; \quad x_{(\lfloor \frac{n}{k} \rfloor - 1)} = x_{k \lfloor \frac{n}{k} \rfloor - 1} \dots x_{k(\lfloor \frac{n}{k} \rfloor - 1)}; \quad x_{(\lfloor \frac{n}{k} \rfloor)} = x_{n-1} \dots x_{k \lfloor \frac{n}{k} \rfloor}. \quad (\text{C2})$$

Among them, $x_{(0)}, x_{(1)}, \dots, x_{(\lfloor \frac{n}{k} \rfloor - 1)}$ are all k -bit numbers, and $x_{(\lfloor \frac{n}{k} \rfloor)}$ are an r -bit number with $r = n - k \lfloor \frac{n}{k} \rfloor$.

Then, we initialize a $(n + k)$ -qubit register as the output qubits. In the i -th step, we add $x_{(i)} \cdot y$ to the result, which is achieved by a sequence of controlled addition as shown in Fig. 17, and get the last k bits m_i . To perform a 2^k -reduction, we use a quantum table introduced in Appendix E 1 to find the appropriate multiples of p , $t_{m_i} p$, such that $t_{m_i} p + m_i \equiv 0 \bmod p$, and add them to the result. Note that after adding $t_{m_i} p$ to the register, the last k bits of the result are all 0, and we can perform a k -bit right shift to achieve a 2^k -reduction. After these steps, we get the result

$$\begin{aligned} & \left(\left((x_{(0)} y/2^k + x_{(1)} y)/2^k + \dots + x_{(\lfloor \frac{n}{k} \rfloor - 1)} y \right) / 2^k + x_{(\lfloor \frac{n}{k} \rfloor)} y \right) / 2^r \bmod p \\ &= \left(x_{(0)} + x_{(1)} 2^k + \dots + x_{(\lfloor \frac{n}{k} \rfloor - 1)} 2^{k(\lfloor \frac{n}{k} \rfloor - 1)} + x_{(\lfloor \frac{n}{k} \rfloor)} 2^{k \lfloor \frac{n}{k} \rfloor} \right) \cdot y/2^n \bmod p \\ &= (x \cdot y)/2^n \bmod p. \end{aligned} \quad (\text{C3})$$

The whole circuit is shown in Fig. 16 and the construction of each building blocks `mul_win` is shown in Fig. 17. It is worth noting that this circuit produces one column of garbage qubits m , which we need to recover later by the reverse operation.

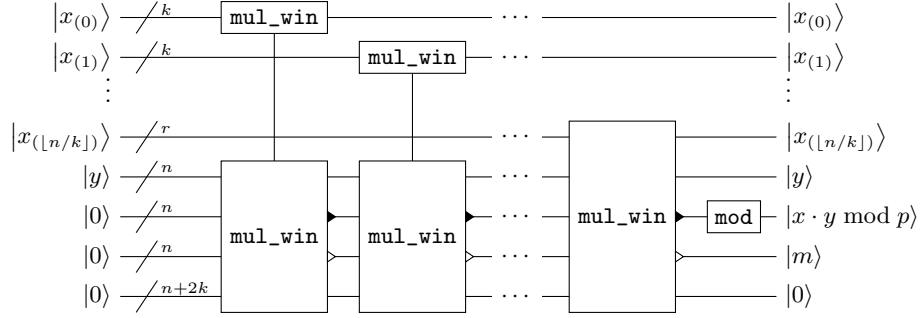


FIG. 16: Quantum circuit for modular multiplication using the windowed trick. The `mul_win` block is shown in 17, and the `mod` block is the modular reduction described in Appendix E3d. The \blacktriangleright and \triangleright represent different outputs of the `mul_win` blocks. The white one \triangleright usually represents the garbage output that needs to be uncomputed, corresponding to the output $|m_i\rangle$ in Fig. 17.

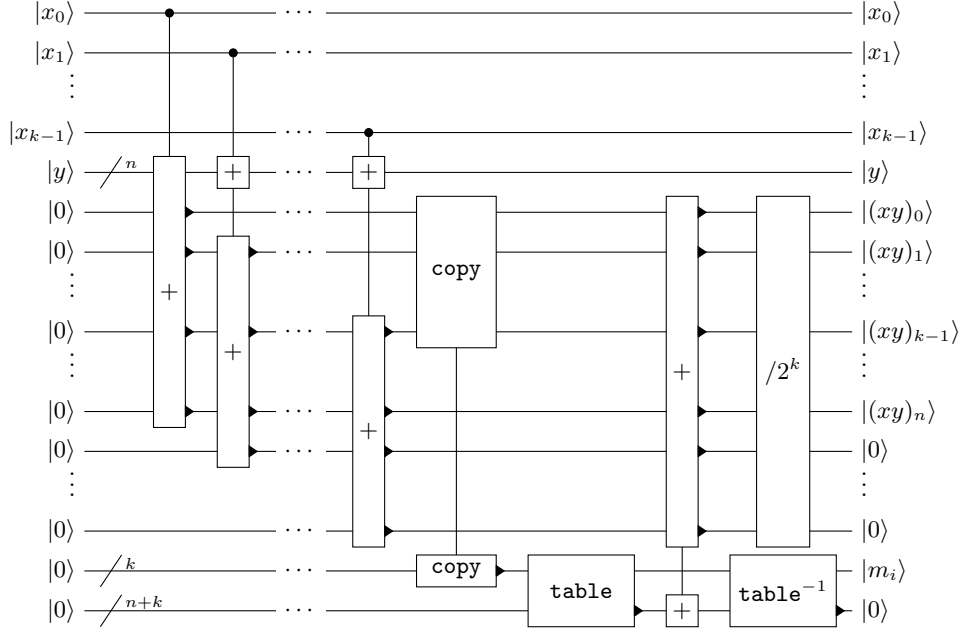


FIG. 17: Quantum circuit for a single `mul_win` operation. `copy` denotes a bit-by-bit CNOT. The “ $/2^k$ ” block denotes a k -bit right shifting operation, as discussed in Appendix E4b. The block `table` is a quantum table that takes a k -bit number m_i as the input and outputs an $(n+k)$ -bit number $t_{m_i}p$, and `table-1` is its inverse, as discussed in Appendix E1.

The parameter k in the windowed trick should be optimized to reduce the Toffoli depth. We conclude that the optimized k is given by $k = \log \log n + o(\log \log n)$ and put the details of the optimization in Appendix D. Specifically, when $n = 256$, we have $k = 3$. As a result, the corresponding Toffoli depth is $2n \log n + 4n \frac{\log n}{\log \log n}$, Toffoli number is $16n^2 + 14 \frac{n^2}{\log \log n}$, CNOT depth is $2n \log n + 12n \frac{\log n}{\log \log n}$, and CNOT number is $4n^2 \frac{\log n}{\log \log n} + \frac{37}{2}n^2$. Note that although the first term $n^2 \frac{\log n}{\log \log n}$ in the CNOT number is asymptotically larger than the Toffoli number, it is even smaller than the second one for practical cases such as $n = 256$. Therefore, we can still regard the leading term as $O(n^2)$.

Finally, we show the layout of qubits used in modular multiplication in Fig. 18. There are totally $10n$ qubits in this figure. Note that since we need to implement an $n+k$ -bit addition, there are k additional qubits for $p_1, p_2, g, a, x \cdot y$, and tp . Furthermore, we need an additional k qubits as input to the table. We store these $5k$ qubits in res . As long

as $n \geq 10$, $n \geq 5k$, and a column of qubits is enough for them. (When $n < 10$, it is not so necessary to use this windowed trick.) Our implementation does not contain a control qubit $ctrl$, as it is not required in our overall point addition. The gate interaction distance is 4, the distance between $|res\rangle$ and the dynamic circuit qubits.

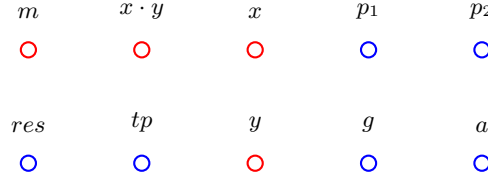


FIG. 18: Qubits layout for modular multiplication. x, y are the input, $x \cdot y, m$ are the real and garbage outputs, respectively. tp stores the number that we get by looking up the table. p_1, p_2, g, a are the qubits for addition. res stores the additional $5k$ qubits for the $n + k$ -bit addition.

It is worth noting that the above circuit, denoted as mul , produces a column of garbage qubits m , which must be cleaned up after the computation. This can be achieved by performing a copy operation followed by the inverse multiplication circuit mul^{-1} . We will denote the whole procedure as mul_F , where the subscript F stands for “full”, as illustrated in Fig. 19a. In our construction of elliptic-curve point addition, the multiply-and-add operation $|x\rangle |y\rangle |z\rangle \mapsto |x\rangle |y\rangle |(z + xy) \bmod p\rangle$ is also frequently used. This operation can be realized through a sequence of mul , $+$, and mul^{-1} operations, and we denote it as mul^+ , as shown in Fig. 19b. Finally, modular squaring $|x\rangle |0\rangle \mapsto |x\rangle |(x^2) \bmod p\rangle$ is implemented in an analogous manner to modular multiplication, as discussed in Appendix E 4 c, while the square-and-subtract operation sq^- is constructed in parallel to mul^+ .

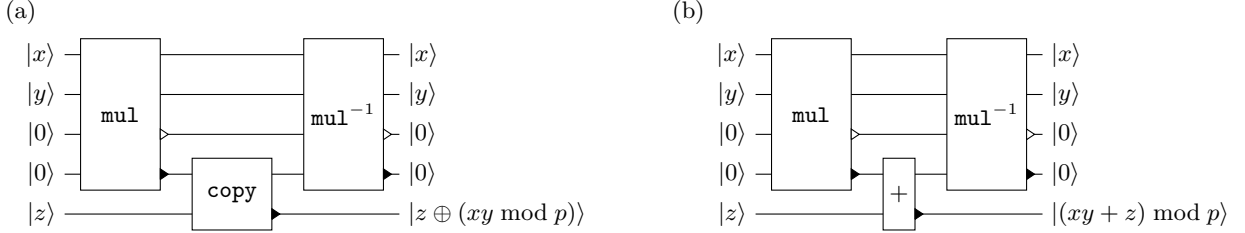


FIG. 19: The quantum circuits for (a) mul_F and (b) mul^+ . copy denotes a bit-by-bit CNOT, and mul^{-1} is the reverse operation of mul .

3. Modular Division

The modular division implements $|x\rangle |y\rangle |0\rangle \mapsto |x\rangle |y\rangle |x^{-1} \cdot y \bmod p\rangle$. The division can be implemented by computing the inversion of y and the multiplying it with x . Thus, we will discuss the modular inversion first.

To ensure consistency with modular multiplication, modular inversion should also be performed in the Montgomery representation. Accordingly, the input and output of the inversion circuit are defined as $x' = (x \cdot 2^n) \bmod p$ and $(x^{-1})' = (x^{-1} \cdot 2^n) \bmod p$, respectively. The classical Montgomery inversion algorithm [51] is provided in Algorithm 6. This algorithm is founded on the Euclidean algorithm, thereby circumventing the logically intricate trial division method, and exclusively employs addition, subtraction, and bit-shift operations, which are well-suited for quantum circuits. The algorithm we present exhibits a subtle distinction from the original algorithm in [51]: we impose that the loop iterates exactly $2n$ times, whereas the original algorithm utilizes a while loop conditioned on $v > 0$. It can be demonstrated that the number of loop iterations k is bounded by $2n$. To ensure consistency in the quantum algorithm, it is imperative to execute the loop for the maximum possible number of iterations. For an effective iteration count k , the Montgomery inversion algorithm ultimately yields a “pseudo-inverse” $(x^{-1} \cdot 2^{n-k}) \bmod p$, which necessitates k doubling operations relative to the correct result $(x^{-1} \cdot 2^n) \bmod p$. This is achieved through a sequence of modular doubling in parallel with the implementation of the Montgomery inversion algorithm. Consequently, k must be stored in a register, and the result must be adjusted accordingly based on k . The quantum implementation [25, 26] is illustrated in Fig. 20 and Fig. 21.

This circuit takes $|x\rangle$ in Montgomery representation as input and produces a “pseudo-inverse” state $|(x^{-1} \cdot 2^{n-k}) \bmod p\rangle$ as output, together with ancillary registers: a $2n$ -qubit garbage register $|l\rangle$, a single-qubit flag $|ctrl'\rangle$, and a $(\lceil \log n \rceil + 1)$ -

qubit counter storing the value of k . In each iteration, the **round** operation is responsible for handling u, v, r, s , while the remaining operations are responsible for handling k . The missing k doublings are later corrected in the inverse operation of the inversion procedure, conditioned on the state of $|ctrl'\rangle$, corresponding to the $doub^k$ operation shown in Fig. 22.

Algorithm 6: classical algorithm for computing Montgomery inversion [25, 26]

Input : $p, x', 0, 1$
Output: $1, 0, (x^{-1})', p, k$

$u \leftarrow p, v \leftarrow (x \cdot 2^n) \bmod p, r \leftarrow 0, s \leftarrow 1, k \leftarrow 0;$
for $i \leftarrow 1 \cdots 2n$ **do**
 if $v > 0$ **then**
 if u *is even* **then**
 $u \leftarrow \frac{u}{2}, s \leftarrow 2s;$
 else if v *is even* **then**
 $v \leftarrow \frac{v}{2}, r \leftarrow 2r;$
 else if $u > v$ **then**
 $u \leftarrow \frac{u-v}{2}, r \leftarrow r+s, s \leftarrow 2s;$
 else
 $v \leftarrow \frac{v-u}{2}, s \leftarrow r+s, r \leftarrow 2r;$
 else
 $r \leftarrow (2r) \bmod p;$
 $k \leftarrow k+1;$
 $r \leftarrow p-r;$
return u, v, r, s, k

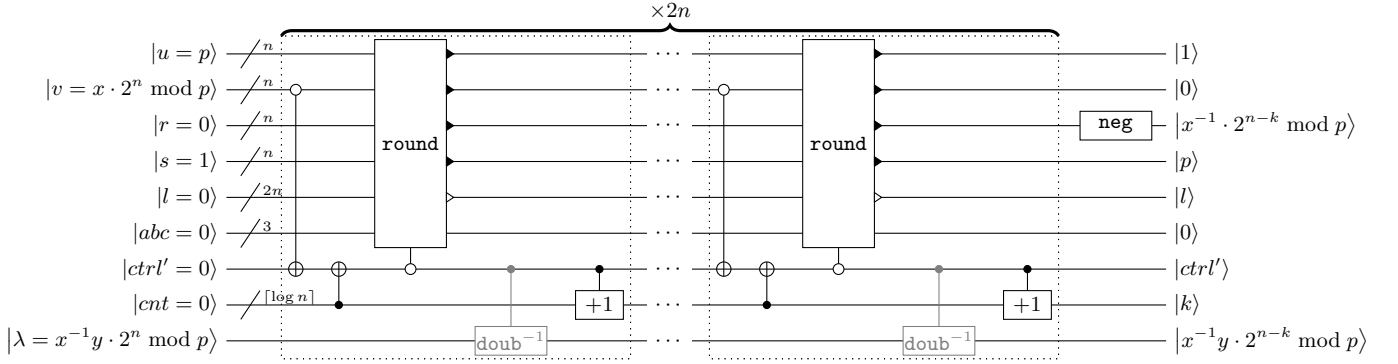


FIG. 20: Quantum circuit for modular inversion. CNOT with multiple control qubits is the AND operation mentioned in Appendix E 2. The $+1$ block is a controlled constant addition of 1. **round** is shown in Fig. 21. $doub^{-1}$ is the controlled doubling operation used to convert the result from a “pseudo-inverse” to a “real-inverse”. $|\lambda\rangle$ is the column of qubit that stores the final result of the modular division, as shown in Fig. 22. This $doub^{-1}$ only occurs at the inverse of modular inversion, so it is denoted in gray here. Also, it functions as the modular doubling in the inverse circuit, so here we use a superscript of -1 to denote it. **neg** is modular negation $|x\rangle \mapsto |p-x\rangle$, as discussed in Appendix E 3 d.

A controlled **round** costs $(3 \log n + 2 \log \log n)$ Toffoli depth, $45n$ Toffoli gates, $(3 \log n + 2 \log \log n)$ CNOT depth, and $56n$ CNOT gates. An inversion costs $(8 \log n + 10 \log \log n)$ Toffoli depth, $88n^2$ Toffoli gates, $(6n \log n + 8n \log \log n)$ CNOT depth, and $112n^2$ CNOT gates. Detailed counting is given in Appendix D.

As mentioned before, modular division consists of modular inversion and modular multiplication, including two modular multiplications, one modular inversion, one modular inversion plus modular doubling, and one copy. The whole circuit is shown in Fig. 22. The circuit design is straightforward. We first perform one inversion and one

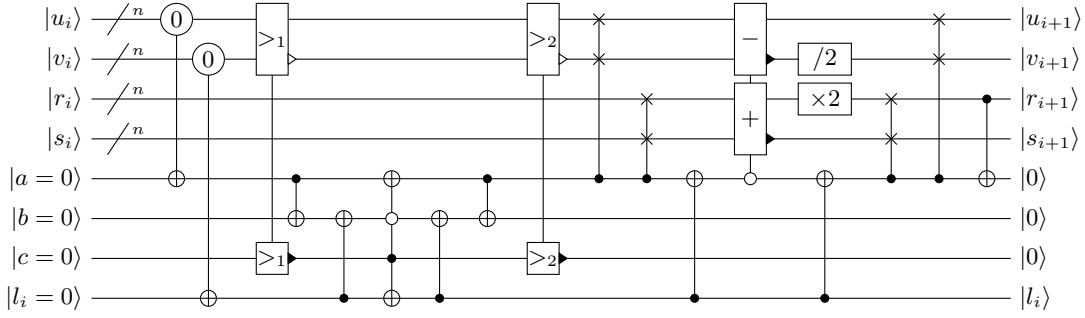


FIG. 21: Quantum circuit for the **round** operation. The first two gates are CNOT gates, where the number “0” in the white circle means that they use the lowest bit of u or v , which denotes the parity, as the control bit, conditional on the lowest bit being $|0\rangle$. $\times 2, /2$ are simply 1-bit shifts given in Appendix E 4 b. $>_1, >_2$ are the half comparators, as discussed in Appendix E 3 c.

multiplication to calculate the result. Then, we copy the result to a clean register and undo the computation. Recall that we should use doubling operations to correct the result. The whole division circuit has $(22n \log n + 8n \frac{\log n}{\log \log n})$ Toffoli depth, $(238n^2 + 28 \frac{n^2}{\log \log n})$ Toffoli gates, $(18n \log n + 24n \frac{\log n}{\log \log n})$ CNOT depth, and $(8n^2 \frac{\log n}{\log \log n} + 309n^2)$ CNOT gates.

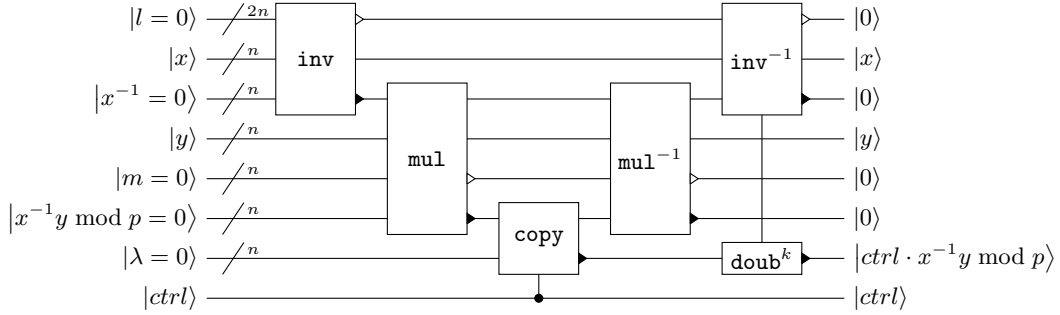


FIG. 22: Quantum circuit for modular division. inv is the modular inversion operation and inv^{-1} is its inverse. mul is the modular multiplication operation and mul^{-1} is its inverse. copy is a bit-to-bit Toffoli controlled by $|ctrl\rangle$. doub^k is the modular doubling given in Appendix E 3 e. It is a sequence of $2n$ modular doublings controlled by a qubit in inv^{-1} , as shown in Fig. 20. Only k of them will be operated, so we denote them as doub^k . Here, the ancillary qubits used for the building block operations are neglected.

For the space cost, our qubit layout of this operation consists of $17n$ qubits. It contains two parts, the inversion part and the multiplication part, as shown in Fig. 23. The gate interaction distance is still 4, the distance between $|res\rangle$ and the dynamic circuit qubits in the multiplication part.

In addition, if we do not allow the parallelization of two additions, we only need $13n$ qubits. As a tradoff, the Toffoli depth will increase to $36n \log n + 8n \frac{\log n}{\log \log n}$.

Appendix D: Detailed Resource Cost Analysis

In this section, we provide a detailed analysis of the resource costs of the circuit, including the Toffoli depth, Toffoli count, CNOT depth, and CNOT count. Since many Toffoli gates in our construction are long-range and are implemented using dynamic circuits, we also evaluate the total qubit number and the corresponding gate interaction distance.

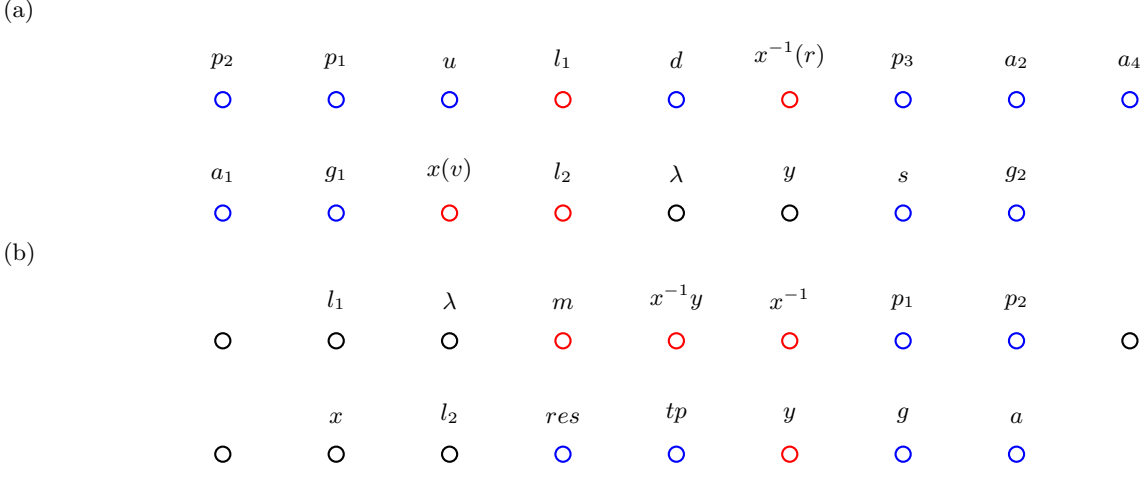


FIG. 23: Qubits layout for modular division. (a) The inversion part. It uses two sets of qubits a_1, p_1, p_2, g_1 and a_2, p_3, p_4, g_2 to implement addition simultaneously. u, v, r, s are four registers in Algorithm 6. l_1, l_2 are the output of $2n$ garbage qubits. d is the column that stores $a, b, c, ctrl'$ and the counter cnt for k in the algorithm. (b) The multiplication part. It has the same components as the normal multiplication shown in Fig. 18, but with different qubit locations. To achieve a lower gate interaction distance, we change the location of l_1 and l_2 by swapping.

1. Modular Addition

The modular addition, as shown in Fig. 13, consists of one controlled addition, one controlled constant addition, one controlled comparator, and one Pauli X gate. The resource cost of all the operations above can be found in Appendix E3. By combining them we can get the resource cost of one controlled modular addition:

$$\begin{aligned}
 \text{Toffoli depth} &\simeq 2 \times (2 \log n + 2 \log \log n) + \log n \simeq 5 \log n + 4 \log \log n, \\
 \text{Toffoli number} &\simeq 16n + 13n + 4n \simeq 33n, \\
 \text{CNOT depth} &\simeq 2 \times (2 \log n + 2 \log \log n) + \log n \simeq 5 \log n + 4 \log \log n, \\
 \text{CNOT number} &\simeq \frac{37}{2}n + \frac{39}{2}n + 4n \simeq 42n.
 \end{aligned} \tag{D1}$$

2. Modular Multiplication

The specific construction of modular multiplication circuit is already discussed in C2. By summing up the cost of each part, the total resource cost of one modular multiplication is

$$\begin{aligned}
\text{Toffoli depth} &\simeq \left\lfloor \frac{n}{k} \right\rfloor (k \cdot (2 \log n + 2 \log \log n) + (2 \log(n+k) + 2 \log \log(n+k)) + 0 + 2 \times (2^k - 1)) \\
&\quad + (r \cdot (2 \log n + 2 \log \log n) + (2 \log(n+r) + 2 \log \log(n+r)) + 0 + 2^r) + (2 \log n + 2 \log \log n), \\
\text{Toffoli number} &\simeq \left\lfloor \frac{n}{k} \right\rfloor (k \cdot 16n + 14(n+k) + 0 + 2 \times (2^k - 1)) + (r \cdot 16n + 14(n+r) + 0 + 2^r) + 12n, \\
\text{CNOT depth} &\simeq \left\lfloor \frac{n}{k} \right\rfloor (k \cdot (2 \log n + 2 \log \log n) + (2 \log(n+k) + 2 \log \log(n+k)) + 1 + 2 \times 2^k \times 5) \\
&\quad + (r \cdot (2 \log n + 2 \log \log n) + (2 \log(n+r) + 2 \log \log(n+r)) + 1 + 3(r+2) + 2^r \times 5) \\
&\quad + (2 \log n + 2 \log \log n), \\
\text{CNOT number} &\simeq \left\lfloor \frac{n}{k} \right\rfloor \left(k \cdot \frac{37}{2}n + 17(n+k) + k + 2 \times 2^k \times (2(n+k) + 1) \right) \\
&\quad + \left(r \cdot \frac{37}{2}n + 17(n+r) + r + 3n(r+1) + 2^r \times (2(n+r) + 1) \right) + \frac{39}{2}n, \\
\text{SWAP depth} &\simeq \left\lfloor \frac{n}{k} \right\rfloor (k+2) + (r+2), \\
\text{SWAP number} &\simeq \left\lfloor \frac{n}{k} \right\rfloor n(k+1) + n(r+1),
\end{aligned} \tag{D2}$$

where k is the window size, which needs to be optimized, and $r = n - k \lfloor \frac{n}{k} \rfloor$ is the number of bits in the last group.

In any of the above equations, the first term represents the cost associated with operations on the k -bit numbers, the second term corresponds to operations on the r -bit number, and the third term accounts for the modular reduction `mod` step. We now focus on the terms within the parentheses of the first term, as the interpretation for the second term follows analogously. Specifically, the first component in the parentheses corresponds to the k controlled additions, the second to a single standard addition, the third to the `copy` operation, and the last to the two quantum table lookups. The SWAP gates originate entirely from the k -bit shift operations. The origin of these quantities are provided in Appendices D1 and E.

To optimize the window size k and achieve the lowest Toffoli depth, we only consider the leading terms of the Toffoli depth. We have $\frac{d}{dk}(2n \log n + \frac{2n}{k}(\log n + 2^k)) = 0$, which gives $k = \frac{1}{\ln 2} \left(W\left(\frac{\log n}{e}\right) + 1 \right)$, where the Lambert W function $y = W(x)$ is the inverse function of $x = f(y) = y \cdot e^y$. When n is sufficiently large, $W(x) \approx \ln x$, implying $k = \log \log n + o(\log \log n)$, and Toffoli depth $\simeq 2n \log n + 4n \frac{\log n}{\log \log n}$. To compare, normal multiplication costs $4n \log n + 4n \log \log n$ Toffoli depth, implying that our windowed skill saves about half the depth. In this case, the Toffoli number is $16n^2 + 14 \frac{n^2}{\log \log n}$, CNOT depth is $2n \log n + 12n \frac{\log n}{\log \log n}$, CNOT number is $4n^2 \frac{\log n}{\log \log n} + \frac{37}{2}n^2$, SWAP depth is n , and SWAP number is n^2 . Again, the additional factor $\frac{\log n}{\log \log n}$ in the CNOT depth and number is negligible in practical cases, since it is approximately a constant in such cases.

3. Modular Division

As shown in Fig. 20 and Fig. 22, we should discuss the resource cost of `round` operation first, whose circuit is shown in Fig. 21. Note that this circuit only shows the uncontrolled version of this circuit, while all `round` operations in division are controlled operations actually. Thus, we should discuss the cost of controlled version.

There are two CNOT gates conditioned on the lowest bits of u and v , respectively, which must be promoted to Toffoli gates to incorporate the control. Second, there are four CNOT gates and one CCNOT gate acting on two output qubits, surrounded by two half-comparator segments. By letting the comparator itself be controlled, these gates no longer need explicit control, since when the control bit is 0, all of these operations have no effect. Third, in the core part of the circuit, two pairs of controlled SWAP operations, one pair of controlled additions, and one pair of controlled bit shifts can be executed in parallel. Moreover, all parallelized controlled operations require only a single GHZ state generation for the control qubit. The two CNOT gates conditioned on l_i do not need to be controlled since l_i is always 0 when $ctrl = 0$ (and the second of these CNOTs can be parallelized with the bit shift). However, the final CNOT must be controlled, thereby becoming a Toffoli gate. The overall resource cost for one controlled round

operation is therefore given by

$$\begin{aligned}
& \text{Toffoli depth} \simeq \log n + 2 \times 1 + (2 \log n + 2 \log \log n) + 3 + 5 \simeq 3 \log n + 2 \log \log n, \\
& \text{Toffoli number} \simeq 3n + 4 \times n + 2 \times 16n + 2 \times 2n + 5 \simeq 43n, \\
& \text{CNOT depth} \simeq \log n + 2 \times 5 + (2 \log n + 2 \log \log n) + 6 + 6 \simeq 3 \log n + 2 \log \log n, \\
& \text{CNOT number} \simeq 4n + 2 \times \left(2n + \frac{7}{2}n\right) + \left(17n + \frac{37}{2}n\right) + \left(2n + \frac{7}{2}n\right) + 5 \simeq 56n,
\end{aligned} \tag{D3}$$

where the first term corresponds to the comparator, the second term corresponds to the four controlled swappings, the third term corresponds to the two controlled additions, the fourth term corresponds to the two controlled bit shifting, and the last term corresponds to the other small terms.

The whole inversion, as shown in Fig. 20, includes $2n$ iterations plus one modular negation. Each iteration comprises four components: an n -bit AND operation, a $(\lceil \log n \rceil + 1)$ -bit AND operation, a controlled **round** operation, and a controlled constant addition of $(\lceil \log n \rceil + 1)$ bits. Consequently, the total resource cost of one inversion can be expressed as

$$\begin{aligned}
& \text{Toffoli depth} \simeq 2n \times (\log n + \log(\lceil \log n \rceil + 1) + (3 \log n + 2 \log \log n) + (2 \log(\lceil \log n \rceil + 1) + 2 \log \log(\lceil \log n \rceil + 1))) \\
& \quad + (2 \log n + 2 \log \log n) \simeq 8n \log n + 10n \log \log n, \\
& \text{Toffoli number} \simeq 2n \times (n + (\lceil \log n \rceil + 1) + 43n + 12(\lceil \log n \rceil + 1)) + 12n \simeq 88n^2, \\
& \text{CNOT depth} = 2n \times (0 + 0 + (3 \log n + 2 \log \log n) + (2 \log(\lceil \log n \rceil + 1) + 2 \log \log(\lceil \log n \rceil + 1))) \\
& \quad + (2 \log n + 2 \log \log n) \simeq 6n \log n + 8n \log \log n, \\
& \text{CNOT number} \simeq 2n \times \left(0 + 0 + 52n + \frac{41}{2}(\lceil \log n \rceil + 1)\right) + 13n \simeq 112n^2,
\end{aligned} \tag{D4}$$

where the first term corresponds to the $2n$ iterative rounds, and the second term corresponds to the final modular negation. Within the parentheses of the first term, the first two items represent the two AND operations, the third term corresponds to the controlled **round** operation, and the final term corresponds to the controlled constant addition.

In the uncomputation of inversion, we need to do the controlled modular doubling at the same time, which can be partly parallelized with the AND function and the comparator in the controlled **round** operation. Therefore, the resource cost of one **round** plus **doub** operation is:

$$\begin{aligned}
& \text{Toffoli depth} \simeq (2 \log n + 2 \log \log n) + 2 \times 1 + (2 \log n + 2 \log \log n) + 3 + 3 \simeq 4 \log n + 4 \log \log n, \\
& \text{Toffoli number} \simeq (3n + 15n) + 4 \times n + 2 \times 16n + 2 \times 2n + 3 \simeq 58n, \\
& \text{CNOT depth} \simeq (2 \log n + 2 \log \log n) + 2 \times 5 + (2 \log n + 2 \log \log n) + 6 + 6 \simeq 4 \log n + 4 \log \log n, \\
& \text{CNOT number} \simeq (0 + 4n + 23n) + 2 \times \left(2n + \frac{7}{2}n\right) + \left(17n + \frac{37}{2}n\right) + \left(2n + \frac{7}{2}n\right) + 5 \simeq 79n,
\end{aligned} \tag{D5}$$

where the first term corresponds to the comparator parallelizing with the modular doubling, the second term corresponds to the four controlled swappings, the third term corresponds to the two controlled additions, the fourth term corresponds to the two controlled bit shifting, and the last term corresponds to the other small terms.

Similar to Equation (D4), the uncomputation of inversion together with the controlled modular doubling costs $(10n \log n + 14n \log \log n)$ Toffoli depth, $118n^2$ Toffoli gates, $(8n \log n + 12n \log \log n)$ CNOT depth, and $158n^2$ CNOT gates.

The whole division circuit, as shown in Fig. 22, consists of one modular inversion, one modular multiplication and its reverse, one bit-to-bit copy, and the uncomputation of inversion together with the controlled modular doubling.

The resource cost of one modular division is thus

$$\begin{aligned}
\text{Toffoli depth} &\simeq (8n \log n + 10n \log \log n) + (10n \log n + 14n \log \log n) + 2 \times \left(2n \log n + 4n \frac{\log n}{\log \log n} \right) + 1 \\
&\simeq 22n \log n + 8n \frac{\log n}{\log \log n}, \\
\text{Toffoli number} &\simeq 88n^2 + 118n^2 + 2 \times \left(16n^2 + 14 \frac{n^2}{\log \log n} \right) + n \simeq 238n^2 + 28 \frac{n^2}{\log \log n}, \\
\text{CNOT depth} &\simeq (6n \log n + 8 \log \log n) + (8n \log n + 12 \log \log n) + 2 \times \left(2n \log n + 12n \frac{\log n}{\log \log n} \right) + 0 \\
&\simeq 18n \log n + 24n \frac{\log n}{\log \log n}, \\
\text{CNOT number} &\simeq 112n^2 + 158n^2 + 2 \times \left(4n^2 \frac{\log n}{\log \log n} + \frac{39}{2} n^2 \right) + 0 \simeq 8n^2 \frac{\log n}{\log \log n} + 309n^2, \\
\text{SWAP depth} &\simeq 0 + 0 + 2 \times n + 0 \simeq 2n, \\
\text{SWAP number} &\simeq 0 + 0 + 2 \times n^2 + 0 \simeq 2n^2,
\end{aligned} \tag{D6}$$

where the first term corresponds to the modular inversion, the second term corresponds to the reverse modular inversion with controlled modular doubling, the third term corresponds to the modular multiplication and its reverse, and the last term corresponds to the bit-to-bit copy. Similar to the multiplication, the additional factor $\frac{\log n}{\log \log n}$ in the CNOT depth and number is approximately a constant in practical cases.

4. Point Addition

A single point addition, as shown in Fig. 6, includes two modular divisions, four modular multiplications, two modular squarings, five modular additions, three controlled modular additions, and one modular negation, among which two controlled modular additions can be parallelized with two modular additions. The resource cost of one point addition is

$$\begin{aligned}
\text{Toffoli depth} &\simeq 2 \times \left(22n \log n + 8n \frac{\log n}{\log \log n} \right) + 6 \times \left(2n \log n + 4n \frac{\log n}{\log \log n} \right) \\
&\simeq 56n \log n + 40n \frac{\log n}{\log \log n}, \\
\text{Toffoli number} &\simeq 2 \times \left(238n^2 + 28 \frac{n^2}{\log \log n} \right) + 6 \times \left(16n^2 + 14 \frac{n^2}{\log \log n} \right) \\
&\simeq 572n^2 + 140 \frac{n^2}{\log \log n}, \\
\text{CNOT depth} &\simeq 2 \times \left(18n \log n + 24n \frac{\log n}{\log \log n} \right) + 6 \times \left(2n \log n + 12n \frac{\log n}{\log \log n} \right) \\
&\simeq 48n \log n + 120n \frac{\log n}{\log \log n}, \\
\text{CNOT number} &\simeq 2 \times \left(8n^2 \frac{\log n}{\log \log n} + 309n^2 \right) + 6 \times \left(4n^2 \frac{\log n}{\log \log n} + \frac{37}{2} n^2 \right) \\
&\simeq 40n^2 \frac{\log n}{\log \log n} + 735n^2, \\
\text{SWAP depth} &\simeq 2 \times 2n + 6 \times n \simeq 10n, \\
\text{SWAP number} &\simeq 2 \times 2n^2 + 6 \times n^2 \simeq 10n^2,
\end{aligned} \tag{D7}$$

where the first term is the two modular divisions, the second term is the four modular multiplications together with the two modular squarings (since their costs are asymptotically same, as shown in Appendix E4), and we neglect the (controlled) modular additions and negation since they are negligible compared to the divisions, multiplications and squarings.

5. Shor's Algorithm

A direct implementation of point addition

$$\frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle |y\rangle |O\rangle \mapsto \frac{1}{2^n} \sum_{x,y=0}^{2^n-1} |x\rangle |y\rangle |xG + yQ\rangle \quad (\text{D8})$$

requires $2n$ point additions, each of which is controlled by a corresponding bit in x or y . Thus, the corresponding Toffoli/CNOT/SWAP depth/number equals to $2n$ times of that of point addition. Moreover, as discussed in Sec. IV B, the windowed trick [26] can be used to reduce the resource costs. With the help of it, we can save $l-1$ point additions each window at the expense of one quantum table storing 2^l possible states, as shown in Fig. 8.

The whole circuit has $\lceil \frac{2n}{l} \rceil$ iterations, each including two modular divisions, three modular multiplications, seven modular additions, five modular negations, and six quantum tables (four of them have $(l-1)$ -bit input and $2n$ -bit output, and the other two have $(l-1)$ -bit input and n -bit output), among which two modular additions can be parallelized, as shown in Fig. 8. Notice that we ignore the fact the quantum table in the last iteration will have smaller input since it will not affect the asymptotic behavior. Thus, the resource cost of the whole circuit is given by

$$\begin{aligned} \text{Toffoli depth} &\simeq \left\lceil \frac{2n}{l} \right\rceil \left(56n \log n + 40n \frac{\log n}{\log \log n} + 6 \times (2^{l-1} - 1) \right), \\ \text{Toffoli number} &\simeq \left\lceil \frac{2n}{l} \right\rceil \left(572n^2 + 140 \frac{n^2}{\log \log n} + 6 \times (2^{l-1} - 1) \right), \\ \text{CNOT depth} &\simeq \left\lceil \frac{2n}{l} \right\rceil \left(48n \log n + 120n \frac{\log n}{\log \log n} + 6 \times 2^{l-1} \times 5 \right), \\ \text{CNOT number} &\simeq \left\lceil \frac{2n}{l} \right\rceil \left(40n^2 \frac{\log n}{\log \log n} + 735n^2 + 4 \times 2^{l-1} \times (4n + 1) + 2 \times 2^{l-1} \times (2n + 1) \right), \\ \text{SWAP depth} &\simeq \left\lceil \frac{2n}{l} \right\rceil 10n, \\ \text{SWAP number} &\simeq \left\lceil \frac{2n}{l} \right\rceil 10n^2, \end{aligned} \quad (\text{D9})$$

where l is the window size. To get the minimum Toffoli depth up to l , we solve the equation $\frac{d}{dl} \left(\frac{2n}{l} (56n \log n + 6 \times 2^{l-1}) \right) = 0$ when only considering leading terms, which gives $l = \frac{W\left(\frac{56}{3e} n \log n\right) + 1}{\ln 2}$, where the Lambert W function $W(x)$ is the root of $t \cdot e^t = x$. When $n = 256$, $l \approx 12.31$. When n is sufficiently large, $W(x) \approx \ln x$, giving $l = \log n + o(\log n)$. Our simulation shows that $l \approx \log n + 5$ for $128 \leq n \leq 16384$. In this case, the Toffoli depth is $112n^2 + 80 \frac{n^2}{\log \log n}$, the Toffoli number is $1144 \frac{n^3}{\log n} + 280 \frac{n^3}{\log n \log \log n}$, the CNOT depth is $96n^2 + 240 \frac{n^2}{\log \log n}$, the CNOT number is $80 \frac{n^3}{\log \log n} + 1490 \frac{n^3}{\log n}$, the SWAP depth is $20 \frac{n^2}{\log n}$, and the SWAP number is $20 \frac{n^3}{\log n}$.

Appendix E: Other Useful Circuits

In this section, we introduce some other useful components used in the circuit construction, including quantum table, unbounded AND and OR function, controlled and/or constant quantum adder, comparator, modular negation, modular reduction, modular doubling, (controlled) swapping and bit shifting, and modular squaring. We summarize the resource cost of all the circuits introduced in Sec. D and Sec. E in Table III and Table IV. The first table is for the cost of Toffoli and CNOT gates, while the second table is for the cost of SWAP gates.

1. Quantum Table

A quantum table is a circuit that writes the corresponding data to the data register according to the contents of the index register, that is

$$\sum_i \alpha_i |i\rangle |0\rangle \mapsto \sum_i \alpha_i |i\rangle |a_i\rangle. \quad (\text{E1})$$

TABLE III: The Toffoli and CNOT cost of all the circuits introduced in Appendix. C and Appendix. E.

operation	Toffoli depth	Toffoli number	CNOT depth	CNOT number
GHZ state preparation	0	0	3	$1.5n$
quantum table ¹	$2^k - 1$	$2^k - 1$	$2^k \cdot 5$	$2^k(2m + 1)$
SWAP	0	0	0	0
controlled SWAP	1	n	5	$3.5n$
k -bit shift	0	0	0	0
controlled 1-bit shift ²	3	$2n$	6	$3.5n$
AND	$\log n$	n	0	0
integer addition ³	$2 \log n + 2 \log \log n$	$14n$	$2 \log n + 2 \log \log n$	$17n$
constant addition	$2 \log n + 2 \log \log n$	$12n$	$2 \log n + 2 \log \log n$	$16n$
controlled addition	$2 \log n + 2 \log \log n$	$16n$	$2 \log n + 2 \log \log n$	$18.5n$
controlled constant addition	$2 \log n + 2 \log \log n$	$13n$	$2 \log n + 2 \log \log n$	$19.5n$
comparator	$\log n$	$3n$	$\log n$	$4n$
modular negation	$2 \log n + 2 \log \log n$	$12n$	$2 \log n + 2 \log \log n$	$16n$
modular addition	$5 \log n + 4 \log \log n$	$31n$	$5 \log n + 4 \log \log n$	$40.5n$
controlled modular addition	$5 \log n + 4 \log \log n$	$33n$	$5 \log n + 4 \log \log n$	$42n$
modular reduction	$2 \log n + 2 \log \log n$	$13n$	$2 \log n + 2 \log \log n$	$19.5n$
controlled modular doubling ⁴	$2 \log n + 2 \log \log n$	$15n$	$2 \log n + 2 \log \log n$	$23n$
modular multiplication ⁵	$2n \log n + 4n \frac{\log n}{\log \log n}$	$16n^2 + 14 \frac{n^2}{\log \log n}$	$2n \log n + 12n \frac{\log n}{\log \log n}$	$4n^2 \frac{\log n}{\log \log n} + 18.5n^2$
controlled round	$4 \log n + 2 \log \log n$	$45n$	$3 \log n + 2 \log \log n$	$56n$
controlled round combined with				
controlled modular doubling	$4 \log n + 4 \log \log n$	$60n$	$4 \log n + 4 \log \log n$	$79n$
modular inversion	$10n \log n + 10n \log \log n$	$92n^2$	$6 \log n + 8 \log \log n$	$112n^2$
modular inversion combined with				
controlled modular doubling	$10n \log n + 14n \log \log n$	$122n^2$	$8 \log n + 12 \log \log n$	$158n^2$
modular division	$24n \log n + 8n \frac{\log n}{\log \log n}$	$246n^2 + 28 \frac{n^2}{\log \log n}$	$18n \log n + 24n \frac{\log n}{\log \log n}$	$8n^2 \frac{\log n}{\log \log n} + 309n^2$
point addition	$60n \log n + 40n \frac{\log n}{\log \log n}$	$588n^2 + 140 \frac{n^2}{\log \log n}$	$48n \log n + 120n \frac{\log n}{\log \log n}$	$40n^2 \frac{\log n}{\log \log n} + 735n^2$
full circuit	$120n^2 + 80 \frac{n^2}{\log \log n}$	$1176 \frac{n^3}{\log n} + 280 \frac{n^3}{\log n \log \log n}$	$96n^2 + 240 \frac{n^2}{\log \log n}$	$80 \frac{n^3}{\log \log n} + 1490 \frac{n^3}{\log n}$

¹ With k bits of input and m bits of output.² We only provide the cost of controlled 1-bit shift since only this controlled shift is used in our circuit.³ The cost of integer subtraction is the same as addition.⁴ There is no uncontrolled modular doubling operation in our circuit. However, one can simply remove the control qubit to achieve it.⁵ The cost of modular squaring is the same as modular multiplication.

TABLE IV: The SWAP cost of all the circuits introduced in Sec. D and Sec. E. For those operation presented in Table III but not presented in this table, their SWAP depth and SWAP number are both 0.

operation	SWAP depth	SWAP number
SWAP	1	1
k -bit shift	$k + 2$	$n(k + 1)$
modular multiplication	n	n^2
modular division	$2n$	$2n^2$
point addition	$10n$	$10n^2$
full circuit	$20 \frac{n^2}{\log n}$	$20 \frac{n^3}{\log n}$

An efficient way for implementing a quantum table is proposed in [32] and shown in Fig. 24, which uses $2^k - 1$ Toffoli gates as well as depth, where k is the size of the index register, and let m be the bit number of the data output.

Intuitively, this circuit accumulates the information in the index through ancillas, and then performs controlled gates on the data qubits using the final ancilla. For example, only when the content in the index is $|000\rangle$, can the ancilla qubit above d_0 be activated, thereby inputting the information of d_0 into the circuit. This way requires using one control qubit to control multiple X gates, which can be efficiently implemented by dynamic circuits. Thus, this circuit can be modified to fit our requirements by adding a column of ancilla qubits for control.

There are 2^k sets of CNOT gates in the ‘‘Data’’ part (d_0, d_1, \dots, d_7 in Fig. 24) and $2^k - 1$ disjoint CNOTs in the ‘‘Index’’ part. Each set in ‘‘Data’’ has $\frac{m}{2}$ parallel CNOT gates, and needs a GHZ state generation of m bits. Since expanding a control bit into a GHZ state of m bits costs 3 CNOT depth and $\frac{3}{2}m$ CNOT number using dynamic circuit

as shown in Fig. 4, a quantum table with k -bit index and m -bit data has a CNOT depth of $2^k + 2^k \times 3 + 2^k = 2^k \times 5$, and a CNOT number of $2^k \frac{m}{2} + 2^k \frac{3}{2}m + 2^k = 2^k(2m + 1)$.

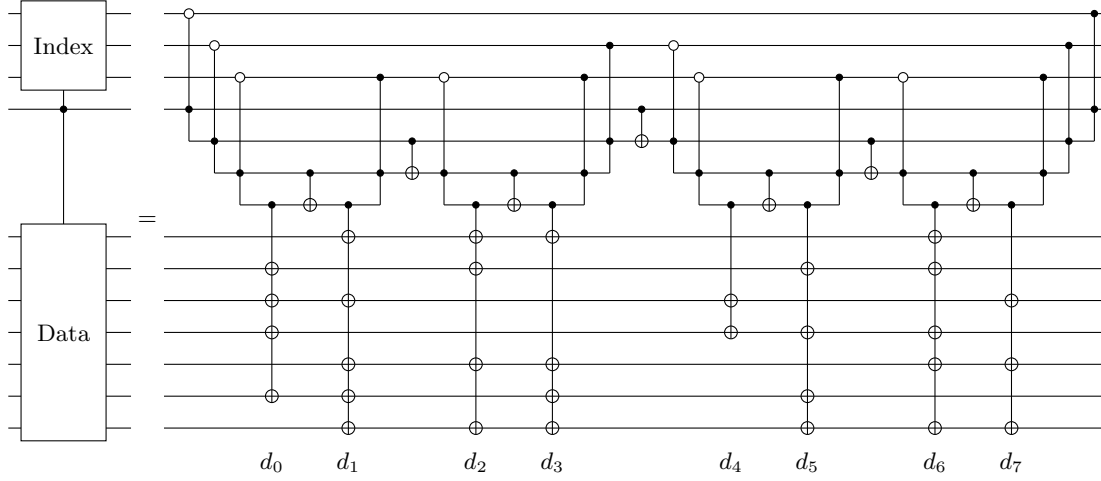


FIG. 24: Quantum circuit for quantum table. On each data qubit, there are multiple controlled- I gates or controlled- X gates, depending on the value of d_i . For example, here $d_0 = (0111010)_2 = 58$.

2. AND and OR Function

An unbounded AND gate is a generalized Toffoli gate with unbounded fan-in, i.e.,

$$\text{AND } |x_1\rangle |x_2\rangle \cdots |x_n\rangle |y\rangle = |x_1\rangle |x_2\rangle \cdots |x_n\rangle \left| y \oplus \prod_{i=1}^n x_i \right\rangle, \quad (\text{E2})$$

where x_1, x_2, \dots, x_n, y are binary numbers. A naive way to implement n -qubit AND function is by using ancillary qubits to record temporary AND results. In the i -th step, we use the i -th data qubit and the $(i-1)$ -th ancillary qubit as control, and the i -th ancillary qubit as target to implement a Toffoli gate ($1 \leq i \leq n$). The final result will accumulate on the n -th ancillary qubit.

To implement an unbounded AND gate using a low-depth quantum circuit with geometric constraint, we put the data qubits and ancillary qubits stated before into two columns, and include another column of ancillary qubits used for dynamic circuits. Here, we let $n = 2^t$ for convenience. Intuitively, in the 0-th step, we divide the data qubits into adjacent groups in pairs, and accumulate the information of each group onto the adjacent ancilla qubit through Toffoli gate. After each step, the ancilla qubits obtained from the previous step will be divided into adjacent groups in pairs, and the information of each group will be accumulated through Toffoli gate onto the unused ancilla qubit located in the middle of them.

More specifically, in the 0-th step, we use the $(2j-1)$ -th and the $(2j)$ -th data qubits as control, and the $(2j-1)$ -th ancilla qubits as target to implement a logical AND gate ($1 \leq j \leq 2^{t-1}$). In the i -th step ($1 \leq i \leq t-1$), we use the $2^{i-1}(4j-3)$ -th and the $2^{i-1}(4j-1)$ -th ancilla qubits as control, and the $2^i(2j-1)$ -th ancilla qubit as target to implement a logical AND gate ($1 \leq j \leq 2^{t-1-i}$). All the long-range Toffoli gates in a step can be implemented simultaneously through disjoint dynamic circuits.

Finally, we need to uncompute the ancilla qubits. This is done through uncomputation gates. Because the Toffoli depth of each step in the first phase is one, and the Toffoli number of the i -th step in the first phase is $n/2^{i+1}$, our AND function has a Toffoli depth $\log n$, Toffoli number n , and no CNOT gates. The OR function can be realized by implementing AND function after applying X gate on each qubit.

3. Variants of addition

In this subsection, we introduce several variants of quantum addition, including (controlled) out-place quantum adder, controlled (constant) in-place quantum adder, quantum negation, quantum comparator, quantum modular

reduction, and (controlled) quantum modular doubling. Except the out-place adder, all these adders are based on the in-place adder shown in Algorithm 3.

a. *Out-place quantum adder*

To achieve an out-place adder $|x\rangle|y\rangle|0\rangle \mapsto |x\rangle|y\rangle|x+y\rangle$, one only need to add x_i, y_i onto the carry bits c_i after it is computed. The algorithm is shown in Algorithm 7. It has $2n$ input qubits, $n+1$ output qubits, s_a ancillary qubits, Toffoli depth $d_t + 1$, Toffoli number $n_t + n$, CNOT depth $d_c + 3$, and CNOT number $n_c + 3n - 1$, where the parameters s_a, d_t, n_t, d_c and n_c are defined in Sec. III B. If we use our carry bit computing method, the leading term of these costs will be

$$\begin{aligned}
& \text{Toffoli depth} = \log n + \log \log n + O(1), \\
& \text{Toffoli number} = 7n + O(1), \\
& \text{CNOT depth} = \log n + \log \log n + O(1), \\
& \text{CNOT number} = \frac{19}{2}n + O(1), \\
& \text{Ancilla} = 3n + O(1).
\end{aligned} \tag{E3}$$

Algorithm 7: quantum algorithm for out-place adder.

Function OutPlaceAdder($x, y; s; a$):

Input : n -qubit number x ; n -qubit number y ; $(n+1)$ -qubit s , initialized to 0; ancilla a (size depends on ComputeCarry), initialized to 0.

Output: x, y, a remain the same; s holds sum bits.

```

1   $s[i+1] \oplus = x[i]y[i]$  for  $i \leftarrow 0, \dots, n-1$ ;           // set  $s[i+1] = g[i, i+1]$ 
2   $y[i] \oplus = x[i]$  for  $i \leftarrow 1, \dots, n-1$ ;           // set  $y[i] = p[i, i+1]$  for  $i \geq 1$ 
3  ComputeCarry( $y; s; a$ );                                     // set  $s[i] = c_i$  for  $i \geq 1$ 
4   $s[i] \oplus = y[i]$  for  $i \leftarrow 0, \dots, n-1$ ;         // set  $s[i] = x_i \oplus y_i \oplus c_i = s_i$  for  $i \geq 1$ 
5   $s[0] \oplus = x[0]$ ;  $y[i] \oplus = x[i]$  for  $i \leftarrow 1, \dots, n-1$ ; // set  $s[0] = s_0$  and recover  $y$  to 0

```

To construct a controlled out-of-place adder, we introduce n additional qubits to serve as the control register. First, we prepare an n -qubit GHZ state to distribute the control, which requires $\frac{3}{2}n$ CNOT gates with a depth of 3. The control qubits then condition the operations in lines 1, 4, and “ $s[0] \oplus x[0]$ ” of Algorithm 7. When the control bit is 0, the sum register s remains in the $|0\rangle$ state after the first line, ensuring that the carry-bit computation does not alter any values and that s stays $|0\rangle$ throughout the computation. For the quantum realization of the controlled first line, the n Toffoli gates are replaced by triple-controlled Toffoli (C^3X) gates. Each C^3X gate can be decomposed into two standard Toffoli gates using one ancilla, resulting in an additional $2n$ Toffoli gates with a depth of 2 and n ancillas in total. This substitution does not increase the overall ancilla requirement. To achieve a T -depth of 1 for these controlled operations, an additional n ancillas are needed for GHZ-state generation of the control register; these qubits can be reused from the ancillas in the carry-bit computation. Let $d_t^o, n_t^o, d_c^o, n_c^o$, and s_a^o denote the Toffoli depth, Toffoli count, CNOT depth, CNOT count, and ancilla space overhead of the uncontrolled out-of-place adder, respectively. Then, the controlled out-place adder has Toffoli depth $d_t^o + 2$, Toffoli number $n_t^o + 2n + 1$, CNOT depth $d_c^o + 2$, CNOT number $n_c^o + \frac{1}{2}n - 1$, and ancilla space overhead s_a^o .

If one of the input numbers is a classical constant, say x , all operations controlled by the qubits of x can be replaced by Pauli- X gates conditioned on the corresponding classical bits of x . Specifically, line 1 of the algorithm reduces to a single CNOT gate controlled by $y[i]$, while lines 2 and 5 simplify to unconditional X gates. In this way, the constant controlled out-place adder has Toffoli depth $d_t^o - 1$, Toffoli number $n_t^o - n$, CNOT depth $d_c^o - 1$, CNOT number $n_c^o - n + 1$, and ancilla space overhead s_a^o .

Finally, for a controlled constant out-place adder, we can just combine the idea of constant out-place adder and the controlled out-place adder. Specifically, we can replace all the operations controlled by the qubits of x by Pauli- X gates conditioned on the classical bits of x . It costs Toffoli depth $d_t^o + 1$, Toffoli number $n_t^o + n$, CNOT depth $d_c^o + 1$, CNOT number $n_c^o - \frac{1}{2}n + 1$, and ancilla space overhead s_a^o .

b. Controlled (constant) in-place quantum adder

Analogous to the construction of the controlled out-of-place adder, the controlled in-place adder can be implemented using GHZ-state preparation to expand the single control qubit into an n -qubit GHZ state. The corresponding circuit operations are then modified to become controlled operations. Specifically, lines 4, 5, 6, and 10 in Algorithm 3 are replaced by their controlled counterparts. When the control bit is 0, the register $|y\rangle$ after line 6 remains identical to its state after line 3. Consequently, the reverse carry-bit computation restores $|c\rangle$ to $|0\rangle$, and $|y\rangle$ is recovered to its input state upon completion. To achieve a T -depth of 1 for these controlled steps, an additional n ancillas are required for GHZ-state generation of the control register. These ancillas can be reused from those allocated for the carry-bit computation. Let d_t^i , n_t^i , d_c^i , n_c^i , and s_a^i denote the Toffoli depth, Toffoli count, CNOT depth, CNOT count, and ancilla space overhead of the uncontrolled in-place adder, respectively. Then, the controlled in-place adder has Toffoli depth $d_t^i + 2$, Toffoli number $n_t^i + 2n - 3$, CNOT depth d_c^i , CNOT number $n_c^i + \frac{3}{2}n + 1$, and ancilla space overhead s_a^i . Notice that the CNOT depth is the same as that of normal in-place adder, since GHZ preparation can be parallelized with other operations.

If one of the input numbers is a classical constant, say x , all operations controlled by the qubits of x can be replaced by Pauli- X gates conditioned on the corresponding classical bits of x . Therefore, we can change line 1, 2, 6, 8 and 9 into simpler operations as that we do for constant out-place quantum adder. In this way, a constant in-place adder has Toffoli depth $d_t^i - 2$, Toffoli number $n_t^i - 2n + 1$, CNOT depth $d_c^i - 1$, CNOT number $n_c^i - n + 3$, and ancilla space overhead s_a^i .

Finally, for a controlled constant in-place adder, we can just combine the idea of the constant in-place adder and the controlled in-place adder. Specifically, we can replace all the operations controlled by the qubits of x by Pauli- X gates conditioned on the classical bits of x . It costs Toffoli depth $d_t^i - 1$, Toffoli number $n_t^i - n$, CNOT depth $d_c^i + 1$, CNOT number $n_c^i + \frac{5}{2}n$, and ancilla space overhead s_a^i .

It is worth noting that in our controlled addition circuit, all parts that need to be controlled comes after line 3 in Algorithm 3, and by that time the carry bits have already been computed. Therefore, if we want to use the highest carry bit of an addition to control this addition itself, we can first compute the carry bits using line 1 to 3, then use the highest carry bit to control the rest of the addition process. This technique is used in our modular addition, modular reduction, and modular doubling circuits, which are discussed in Appendices C1, E3d, and E3e, respectively, in which we use $(-p)_1$ to represent line 1 to 3 of a controlled $-p$ circuit, and $(-p)_2$ to represent line 4 to 10 of a controlled $-p$ circuit. In this way, we save a constant addition in these circuits compared with [25, 26].

c. Comparator

A comparator implements the transformation $|x\rangle|y\rangle|0\rangle \mapsto |x\rangle|y\rangle|z\rangle$, where $z = 1$ if $x > y$ and $z = 0$ otherwise. To determine whether $x < y$, it suffices to evaluate the sign bit of $x' + y$, where x' denotes the bitwise complement of x . This task can be efficiently accomplished using our carry-bit computation method. To be specific, let $k = \lceil \log n \rceil$. We first extend both x and y to 2^k bits and compute the complementary x' , and then compute the most significant carry bit of $x' + y$, which indicates the comparison result. Since we only need the most significant carry bit, directly using the carry-lookahead algorithm based on Brent-Kung tree proves more efficient. This operation can be performed with a Toffoli depth of k , as it requires only the P_1 and G_1 stages of Algorithm 4. Moreover, since the bits beyond the n -th position are all zeros, this part of the circuit can be substantially simplified.

The algorithm is shown in Algorithm 8. It has $2n$ input qubits, one output qubit, and $4n - \lceil \log(n-1) \rceil - 3$ ancillas. Stage P and G have the same function as stage P_1 and G_1 in the previous Brent-Kung-tree-based method. Line 2, stage P , and stage G use logical AND gates, and line 13, stage P^{-1} , and stage G^{-1} use uncomputation gates (uncomputation gates of G^{-1} costs n ancillas).

Stage P costs $n - \lceil \log(n-1) \rceil - 2$ Toffolis in depth $\lceil \log(n-1) \rceil$, and stage G costs $n - 1$ Toffolis in depth $\lceil \log(n-1) \rceil + 1$. Parallelizing these two stages using the first method discussed in Appendix B1 will require $2(n - \lceil \log(n-1) \rceil - 2)$ CNOT gates in depth $\lceil \log(n-1) \rceil + 1$. In conclusion, the circuit parameters are

$$\begin{aligned}
 \text{Toffoli depth} &= 1 + \lceil \log(n-1) \rceil + 1 = \lceil \log(n-1) \rceil + 2 = \log n + O(1), \\
 \text{Toffoli number} &= n + n - \lceil \log(n-1) \rceil - 2 + n - 1 = 3n - \lceil \log(n-1) \rceil - 3 = 3n + O(1), \\
 \text{CNOT depth} &= 2 + \lceil \log(n-1) \rceil + 1 = \lceil \log(n-1) \rceil + 3 = \log n + O(1), \\
 \text{CNOT number} &= 2n - 2 + 2(n - \lceil \log(n-1) \rceil - 2) = 4n - 2 \lceil \log(n-1) \rceil - 6 = 4n + O(1). \\
 \text{Ancilla} &= 4n - \lceil \log(n-1) \rceil - 3 = 4n + O(1).
 \end{aligned} \tag{E4}$$

Changing this comparator into the controlled version is straightforward. After we computed $G[n]$, we only need to add single Toffoli gate controlled by $G[n]$ and the control bit to determine whether the final output bit is $G[n]$ or 0.

Algorithm 8: quantum algorithm for the comparator.

Function Comparator($x, y; G[n]; G[1 : n - 1], P, a$):

Input : n -qubit number x ; n -qubit number y ; n -qubit string G , $(n - \lfloor \log(n - 1) \rfloor - 2)$ -qubit string P , $2n$ -qubit ancilla a , all initialized to 0.

Output: P_0, a remains the same; G holds carry bits $c_i = g[0, i]$; P holds propagation states, including $p[0, i]$.

```

1   $x[i] = -x[i]$  for  $i \leftarrow 0, \dots, n - 1$ ; // set  $x$  to  $x'$ 
2   $G[i + 1] \oplus = x[i]y[i]$  for  $i \leftarrow 0, \dots, n - 1$ ; // set  $G[i + 1] = g[i, i + 1]$ 
3   $y[i] \oplus = x[i]$  for  $i \leftarrow 1, \dots, n - 1$ ; // set  $y[i] = p[i, i + 1]$ 
4  for  $t \leftarrow 1, \dots, \lfloor \log n \rfloor$ ; // set  $G = c_i = g[0, i]$  for  $x'$  and  $y$ 
5  do
6  |    $P_t[m] = P_{t-1}[2m] \cdot P_{t-1}[2m + 1]$  for  $m \leftarrow 0, \dots, \lfloor 2^{\lfloor \log n \rfloor} / 2^t \rfloor$ ; // stage  $P$ ; some of them may be
   |   unnecessary
7  |    $G[2^t m + 2^t] \oplus = G[2^t m + 2^{t-1}] \cdot P_{t-1}[2m + 1]$  for  $m \leftarrow 0, \dots, \lfloor 2^{\lfloor \log n \rfloor} / 2^t \rfloor$ ; // stage  $G$ ; some of them may be
   |   unnecessary
8  for  $t \leftarrow \lfloor \log n \rfloor, \dots, 1$ ; // recover  $G$  and  $P$  except  $G[n]$ 
9  do
10 |    $G[2^t m + 2^t] \oplus = G[2^t m + 2^{t-1}] \cdot P_{t-1}[2m + 1]$  for  $m \leftarrow 0, \dots, \lfloor 2^{\lfloor \log n \rfloor} / 2^t \rfloor - 1$ ; // stage  $G^{-1}$ ; some of them
   |   may be unnecessary
11 |    $P_t[m] = P_{t-1}[2m] \cdot P_{t-1}[2m + 1]$  for  $m \leftarrow 0, \dots, \lfloor 2^{\lfloor \log n \rfloor} / 2^t \rfloor$ ; // stage  $P^{-1}$ ; some of them may be
   |   unnecessary
12  $y[i] \oplus = x[i]$  for  $i \leftarrow 1, \dots, n - 1$ ; // recover  $y$  to input
13  $G[i + 1] \oplus = x[i]y[i]$  for  $i \leftarrow 0, \dots, n - 1$ ; // recover  $G$  to 0 except  $G[n]$ 
14  $x[i] = -x[i]$  for  $i \leftarrow 0, \dots, n - 1$ ; // recover  $x$  to input

```

Then we do some extra uncomputation in stage G^{-1} to recover $G[n]$ to 0. This will not introduce new Toffolis, as they are all uncomputation gates. Denote the Toffoli depth, number, CNOT depth, number, and ancilla space overhead of the (uncontrolled) comparator as d_t^c , n_t^c , d_c^c , n_c^c , and s_a^c . The controlled comparator has Toffoli depth $d_t^c + 1$, Toffoli number $n_t^c + 1$, CNOT depth d_c^c , CNOT number n_c^c , and ancilla space overhead $s_a^c + 1$. The circuit is shown in Fig. 25.

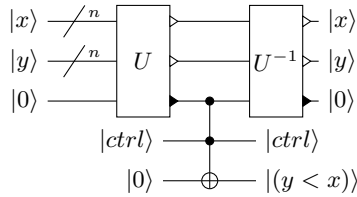


FIG. 25: Quantum circuit for controlled comparator. Here, U is the forward computation process, corresponding to Line 1–7 in Algorithm 8. An example of the details of U can be found in [29].

If one of the input numbers is a constant, say x , all operations controlled by the qubits of x can be replaced by Pauli- X gates conditioned on the corresponding classical bits of x . We can change line 1, 2, 3, 12, 13 and 14 into simpler operations. In this way, a constant controlled comparator has Toffoli depth $d_t^c - 1$, Toffoli number $n_t^c - n + 1$, CNOT depth $d_c^c - 2$, CNOT number $n_c^c - 2n + 2$, and ancilla space overhead s_a^c . A controlled constant comparator can be constructed in the same way, costing Toffoli depth d_t^c , Toffoli number $n_t^c - n + 2$, CNOT depth $d_c^c - 2$, CNOT number $n_c^c - 2n + 2$, and ancilla space overhead $s_a^c + 1$.

We denote the comparator by “ $>$ ”. To reduce circuit depth, it is sometimes advantageous to use only half of the (controlled) comparator, defined as $|x\rangle |y\rangle |0\rangle \mapsto |\bar{x}\rangle |\tilde{y}\rangle |z\rangle$, where $|\tilde{y}\rangle$ represents an intermediate state. This allows one to perform subsequent operations before uncomputing the intermediate registers to restore the original state. We refer to these two halves of the comparator, executed in temporal order, as “ $>_1$ ” and “ $>_2$ ”, respectively, while the full comparator is still denoted by “ $>$ ”.

d. *Modular negation and reduction*

For modular negation $|x\rangle \mapsto |-x \bmod p\rangle = |p - x\rangle$, we first turn x into $-x$, which consists of a bit flip and a “+1”. Next, we do a “+ p ”. To sum up, we need to do a bit flip and a “+ $(p + 1)$ ”, thus its cost is the same as one constant addition.

The modular reduction operation performs $|x\rangle |0\rangle \mapsto |x \bmod p\rangle |x \geq p\rangle$ for $x < 2p$, and is denoted as *mod*. This operation produces an additional garbage bit, which should be uncomputed in subsequent steps. The corresponding quantum circuit is illustrated in Fig. 26. Similar to the modular addition circuit, only one controlled constant addition is required. That’s because the control bit, i.e., the leading carry bit of $x + y - p$, is determined prior to the application of any controlled operations. Consequently, the resource cost of the modular reduction circuit is equivalent to that of a single controlled constant addition.

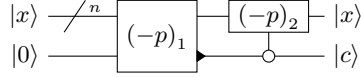


FIG. 26: Quantum circuit for modular reduction. “ $-p$ ” denotes controlled constant subtraction of p where “ $(-p)_1$ ” and “ $(-p)_2$ ” are the two parts of one controlled constant subtraction, as explained in Appendix E 3 b.

e. *Controlled Modular Doubling*

The modular doubling operation, $|x\rangle \mapsto |(2x) \bmod p\rangle$, can be implemented using a circuit structure similar to that of modular addition. The main difference is that the ordinary addition is replaced by a single-bit left shift, and the ancillary qubits can be recovered by checking the parity of the final result. We denote this operation as *doub* to distinguish it from the simple left-shift operation ($\times 2$). This circuit requires one 1-bit left shift, one constant addition, and one controlled constant addition. Accordingly, it has a Toffoli depth of $3 + 2 \log n + 2 \log \log n + 1 \simeq 2 \log n + 2 \log \log n$, a Toffoli count of $2n + 13n = 15n$, a CNOT depth of $6 + 2 \log n + 2 \log \log n \simeq 2 \log n + 2 \log \log n$, and a CNOT count of $\frac{7}{2}n + \frac{39}{2}n = 23n$. The corresponding circuit layout is shown in Fig. 27.

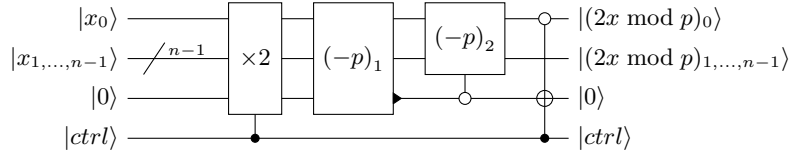


FIG. 27: Quantum circuit for modular doubling. “ $\times 2$ ” denotes a controlled 1-bit left shift, and “ $-p$ ” denotes controlled constant subtraction of p where “ $(-p)_1$ ” and “ $(-p)_2$ ” are the two parts of one controlled constant subtraction, as explained in Appendix E 3 b.

4. Other operations

a. *(Controlled) Swapping*

A SWAP gate, as mentioned previously, is considered a native operation. However, a controlled SWAP cannot be implemented directly and must be decomposed into two CNOT gates and one Toffoli gate, as illustrated in Fig. 28. For a controlled swap between two n -qubit registers, $|x\rangle |y\rangle \mapsto |y\rangle |x\rangle$, we first generate an n -qubit GHZ state from the control qubit, which requires $\frac{3}{2}n$ CNOT gates with a CNOT depth of 3. The middle layer of CNOT gates in the SWAP circuit is then replaced by Toffoli gates. As a result, the total cost is n Toffoli gates and $\frac{7}{2}n$ CNOT gates, with a Toffoli depth of 1 and a CNOT depth of 5. If $|y\rangle = |0\rangle$, the first layer of CNOT gates can be omitted, reducing the CNOT depth by 1 and the total CNOT count by n .

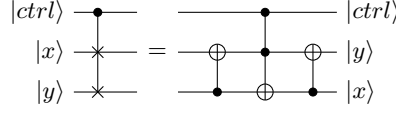
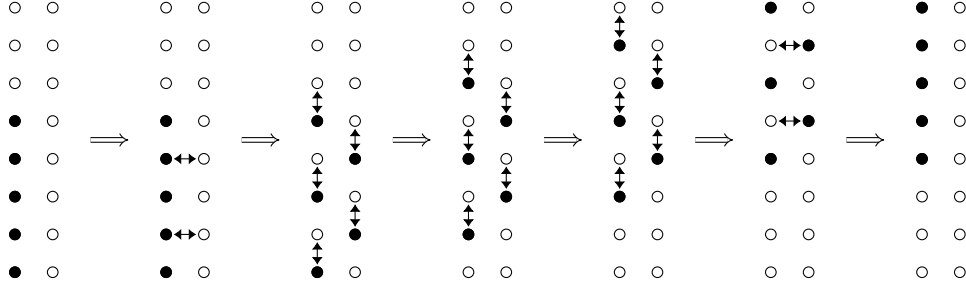


FIG. 28: Quantum circuit for controlled swapping.

b. (Controlled) Shifting

A bit shift of k positions on an n -qubit register can be implemented using $n(k+1)$ SWAP gates with a SWAP depth of $k+2$, as illustrated in Fig. 29. For a controlled bit shift, the control qubit is first expanded into an $(n+k)$ -qubit GHZ state via a dynamic circuit, which requires a CNOT depth of 3 and $\frac{3}{2}(n+k)$ CNOT gates. The subsequent controlled SWAP operations are then performed using this GHZ state control. We do not provide an exact gate count for arbitrary k , since our circuit design only employs controlled 1-bit shifts. A controlled single-bit shift incurs a Toffoli depth of 3, a Toffoli count of $2n$, a CNOT depth of $1+2+3=6$, and a CNOT count of $2n + \frac{3}{2}(n+1) \simeq \frac{7}{2}n$. For convenience, we denote a k -bit left shift as $\times 2^k$ and a k -bit right shift as $/2^k$.

FIG. 29: Quantum circuit for a 3-bit shifting for a 5-bit register. Black points are qubits with data, and white points are ancillas. \leftrightarrow denotes a swapping.

c. Modular Squaring

The overall circuit structure of modular squaring $|x\rangle|0\rangle \mapsto |x\rangle|x^2 \bmod p\rangle$ is the analog to that of modular multiplication, as shown in Fig. 16. The only difference is that we should replace the subroutine `mul_win` by `sq_u_win`, which is shown in Fig. 30. This modification introduces additional CNOT gates compared to modular multiplication, resulting in the following CNOT cost:

$$\begin{aligned}
 \text{CNOT depth} &\simeq \left\lfloor \frac{n}{k} \right\rfloor \left(k \cdot (2 \log n + 2 \log \log n) + (2 \log(n+k) + 2 \log \log(n+k)) + 1 + 2 \times 2^k \times 5 + (2k-1) \right) \\
 &\quad + (r \cdot (2 \log n + 2 \log \log n) + (2 \log(n+r) + 2 \log \log(n+r)) + 1 + 3(r+2) + 2^r \times 5 + (2r-1)) + 11, \\
 \text{CNOT number} &\simeq \left\lfloor \frac{n}{k} \right\rfloor \left(k \cdot \frac{37}{2}n + 17(n+k) + k + 2 \times 2^k \times (2(n+k) + 1) + 2k \right) \\
 &\quad + \left(r \cdot \frac{37}{2}n + 17(n+r) + r + 3n(r+1) + 2^r \times (2(n+r) + 1) + 2r \right) + \frac{39}{2}n,
 \end{aligned} \tag{E5}$$

where the meaning of all terms is the same as Equation D2 except for the last term in the parenthesis, which stands for the additional CNOTs. The Toffoli and SWAP costs do not change, so the optimal window size k is still $\log \log n + o(\log \log n)$, and the corresponding Toffoli and SWAP costs remain the same as modular multiplication, but the CNOT depth will be $2n \log n + 12n \frac{\log n}{\log \log n}$, CNOT number is $4n^2 \frac{\log n}{\log \log n} + \frac{37}{2}n^2$ (asymptotically same with modular multiplication).

where all terms have the same meaning as in Eq. D2, except for the final terms in parentheses, which account for the additional CNOT gates introduced by squaring. The Toffoli and SWAP costs remain unchanged from the modular multiplication circuit. Consequently, the optimal window size is still $k = \log \log n + o(\log \log n)$, and the corresponding Toffoli and SWAP costs are identical to those of modular multiplication. The asymptotic CNOT

costs, however, become CNOT depth = $2n \log n + 12n \frac{\log n}{\log \log n}$ and CNOT count = $4n^2 \frac{\log n}{\log \log n} + \frac{37}{2}n^2$, which are asymptotically equivalent to the modular multiplication results.

The modular squaring circuit requires fewer qubits than modular multiplication, as the $|y\rangle$ register is no longer needed. In total, it uses $9n$ qubits, with a gate interaction distance of 5 for the bi-layer layout and 7 for the single-layer layout.

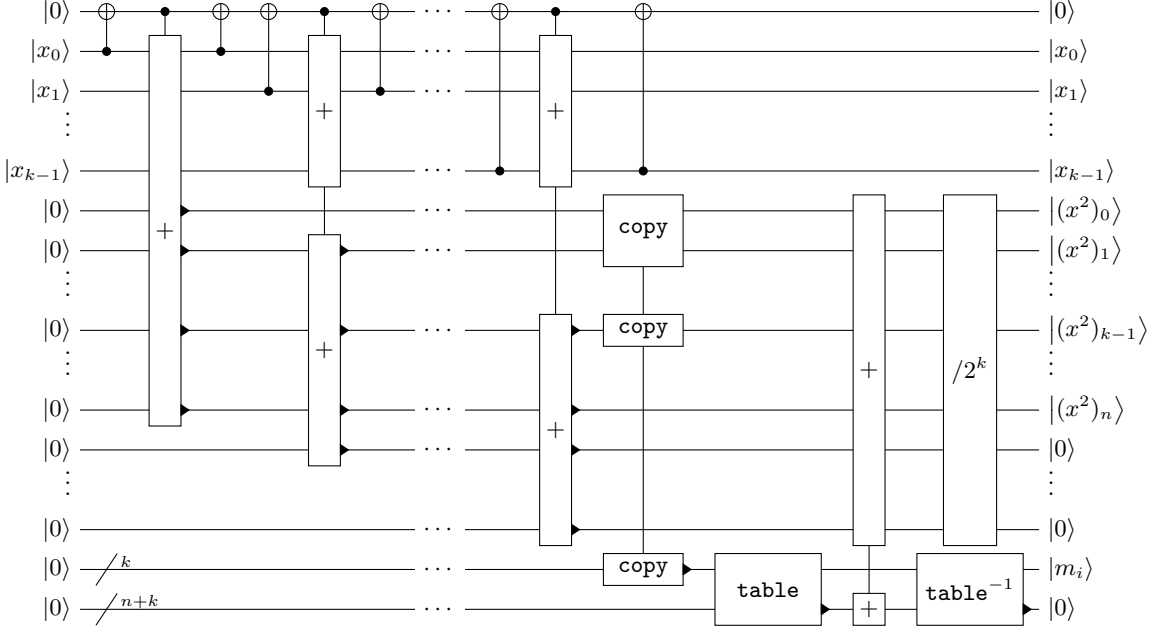


FIG. 30: Quantum circuit for a single `squ_win` operation, similar to Fig. 17.

Appendix F: Single-layer Layout

Since bi-layer qubit layouts are not yet widely adopted in current quantum hardware architectures, we also provide an alternative single-layer realization. To minimize the gate interaction distance, the two columns of qubits in the bi-layer layout are interleaved side by side in the single-layer arrangement. The corresponding layouts for the main circuit operations are illustrated in Fig. 31. A comparison of the maximum gate interaction distances for the bi-layer and single-layer layouts is summarized in Table V. As shown in the table, the interaction distance in the single-layer configuration is approximately twice that of the bi-layer layout, which is consistent with our intuition and geometric expectations.

TABLE V: Gate interaction distance of bi-layer and single-layer layouts for different operations

operation	bi-layer	single-layer
addition	2	3
multiplication	4	7
division	4	7
whole circuit	4	7

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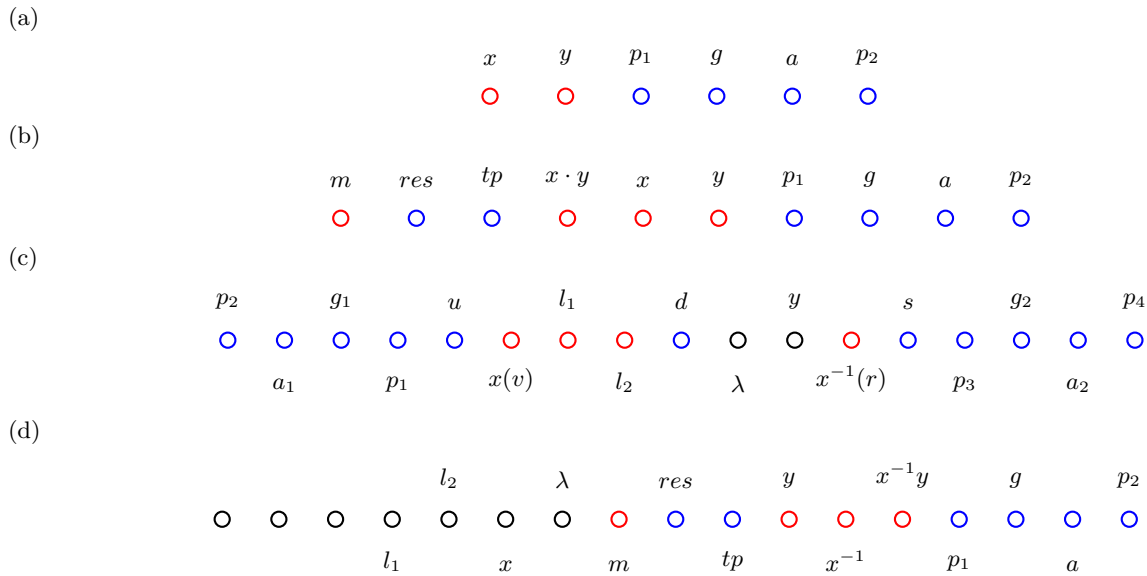


FIG. 31: Single-layer layout for (a) modular addition, (b) modular multiplication, (c) modular division (inversion part), and (d) modular division (multiplication part). The meaning of each column is explained in Fig. 14, Fig. 18 and Fig. 23.

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